

# GREENPAK™

## INTRODUCTION

18. APRIL 2024

MUHAMMAD A. MATEEN

SENIOR FIELD APPLICATION ENGINEER

POWER & ANALOG PRODUCTS

RENESAS ELECTRONICS CORPORATION

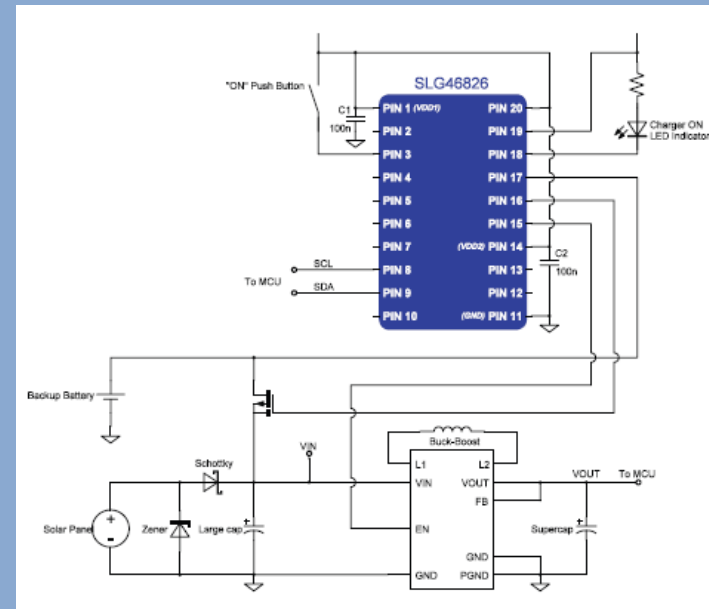
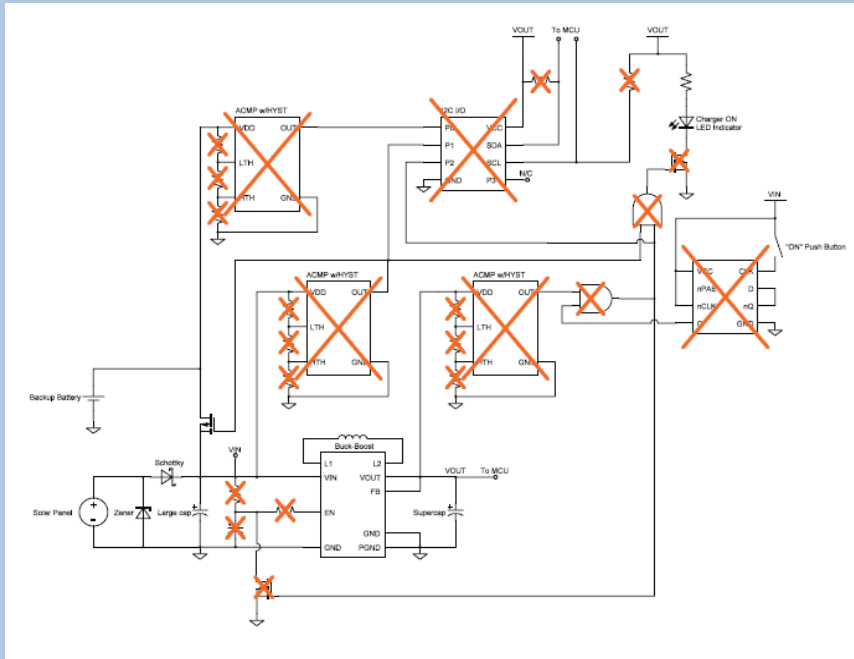
# AGENDA

---

- What is GreenPAK?
- *GreenPAK Development Boards*
- *GreenPAK Simulation Software*
- Designing with *GreenPAK*
- *GreenPAK Macro Cells (Examples)*
- *GreenPAK Resources*
- Design Security
- Wrap-Up

# WHAT IS GREENPAK™? – A CONCEPTUAL APPROACH

## Configurable Mixed-Signal IC



Design reduced by:

- 5 ICs
- 2 NMOS transistors
- 14 passive components

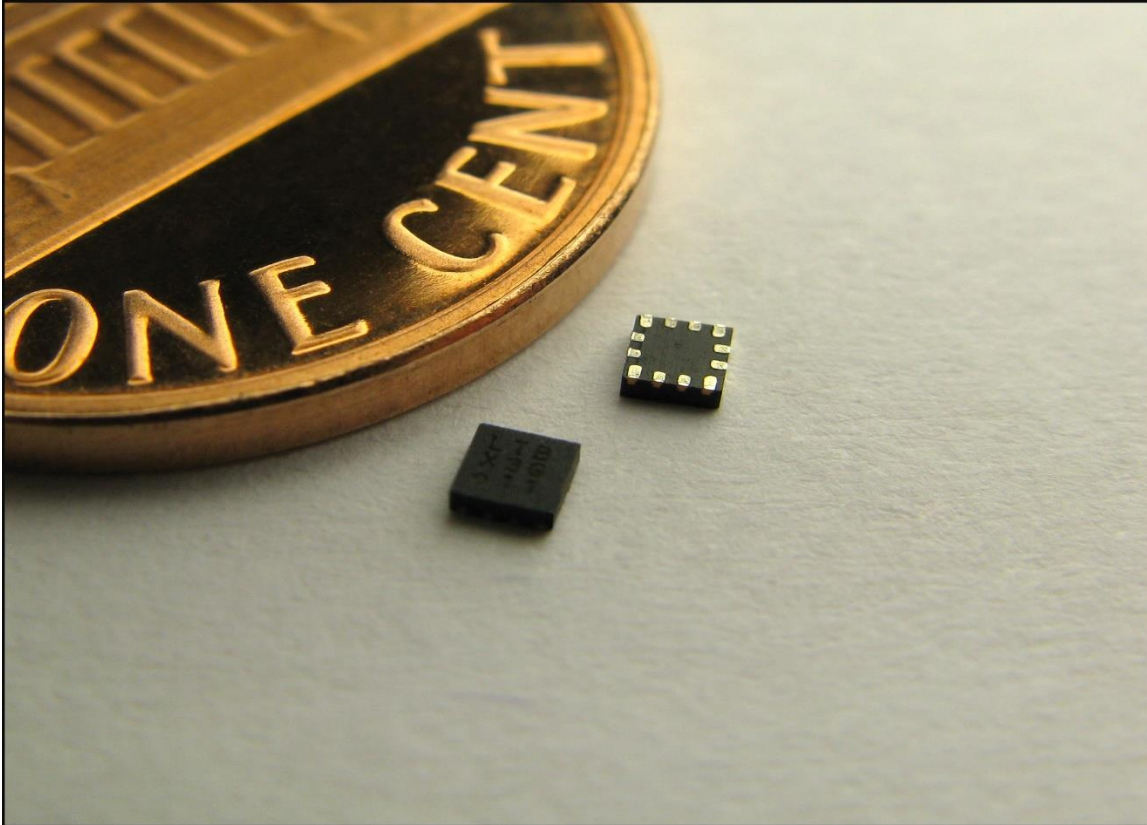
Customer Benefits:

- Integration
- Configurability
- Reliability
- Safety
- Lower power consumption

# WHAT IS GREENPAK?

---

The World's 1<sup>st</sup> Custom Mixed-signal IC (CMIC) Family



- Roughly 60 ICs, each with a unique set of features
- Customizable with simple, free software
- Very small package, down to 1.2mm<sup>2</sup>
- Low power solution
- Can be used in a myriad of applications...

# GREENPAK

Integrate Many System Functions to Minimize Components,  
Reduce PCB Space, and Lower Power

## GreenPAK is ideal for

- Functional replacement of popular mixed-signal standard products and stand-alone discrete circuits
- Providing reliable hardware supervisory functions for devices such as SoCs and Microcontrollers



Design in  
minutes  
Prototype  
in hours



No  
NRE



No Production  
Commitment



14 Week  
Production  
Lead-time



Custom  
Datasheet

## Easy & fast development tools

- GUI-based GreenPAK Designer software
- Development Kits for circuit emulation and IC programming



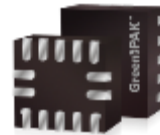
1.0 mm x 1.2 mm  
0.4 mm pitch  
STQFN  
8-pin package



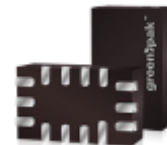
1.6 mm x 1.6 mm  
0.4 mm pitch  
STQFN  
12-pin package



1.6 mm x 2.0 mm  
0.4 mm pitch  
STQFN  
14-pin package



2.0 mm x 2.2 mm  
0.4 mm pitch  
STQFN  
14-pin package



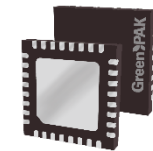
1.6 mm x 2.5 mm  
0.4 mm pitch  
STQFN  
14-pin package



2.0 mm x 3.0 mm  
0.4 mm pitch  
STQFN  
20-pin package



2.0 mm x 2.2 mm  
0.4 mm pitch  
MSTQFN  
22-pin package



4.0 mm x 4.0 mm  
0.4 mm pitch  
STQFN  
32-pin package

# WHAT ARE KEY BENEFITS OF GREENPAK?

---

- **Faster time to market** – Average lead time is **8-weeks for production qty.** Sample qty in 14 days
  - Parts are preprogrammed (Assembly bank) -> Customer parts are programmed, tested, marked accordingly, & packaged -> shipped out to customer
- **Adaptable & flexible design**
- **Design security**
  - Parts can be locked -> Black Box from outside
  - Customer specific part number & custom datasheet -> part number can only be ordered by customer owning part number
- **BOM & design size reduction**
- **Lower cost consideration for designs**
  - No coding required
  - No additional costs for programming
  - MOQ is one reel (3k or 6k parts; depending on Greenpak part)

# A WIDE FAMILY OF PRODUCTS FOR MANY APPLICATIONS

## Overview of Existing Subfamilies

### GreenPAK

- Dual Supply GreenPAK
- GreenPAK with Load Switches
- GreenPAK with Asynchronous State Machine
- GreenPAK with Low Drop Out Regulators
- GreenPAK with In-System Programmability
- PN\*: SLG46xxx and SLG47xxx

[More Info](#)

### HVPAK

- Programmable Mixed-Signal ASIC with High Voltage Features
- Integrated High Voltage up to 26.4 V and High Current up to 3 A Output Drivers
- PN: SLG471xx

[More Info](#)

### Automotive GreenPAK

- Cost-effective NVM programmable devices allowing to integrate many system functions into a single AEC-Q100 qualified IC
- PN: SLG46xxx-A

[More Info](#)

### AnalogPAK

- Programmable Mixed-Signal ASIC with Analog Features
- Rich set of analog blocks (OpAmp's, digital rheostats, etc.)
- MTP NVM with in-system programmability
- PN: SLG470xx

[More Info](#)

### PowerPAK

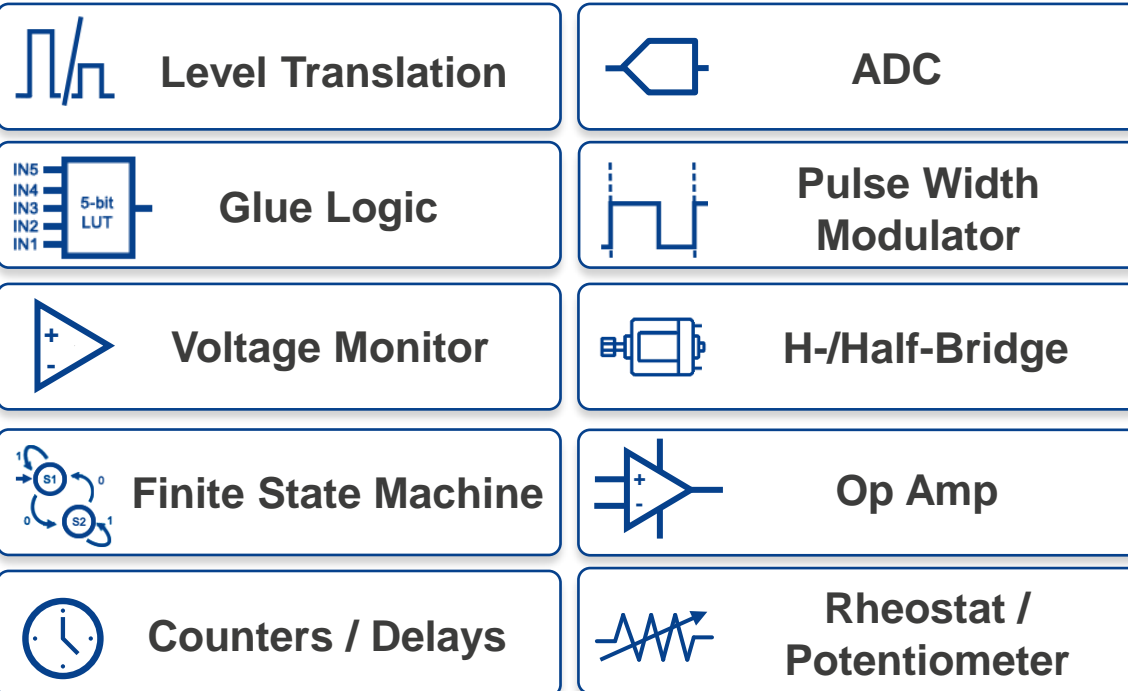
- High PSRR, low noise multi-output LDO IC for advanced camera and sensor systems
- PN: SLG5100x

[More Info](#)

\* PN stands for part number

# WHAT CAN I DO WITH GREENPAK™?

## GreenPAK Functions



## Example Applications

- Supervisory Circuits
- System Reset
- LED Control
- Motor & Fan Control
- Power Sequencing
- Voltage Detection
- Frequency Detection
- Sensor Interface
- Port Detection
- Temperature Control
- Battery Monitor
- See [COOKBOOK](#) for more!

*\*Not for Automotive qualified GreenPAK*

★ Multiple functions & applications can be combined into one IC ★

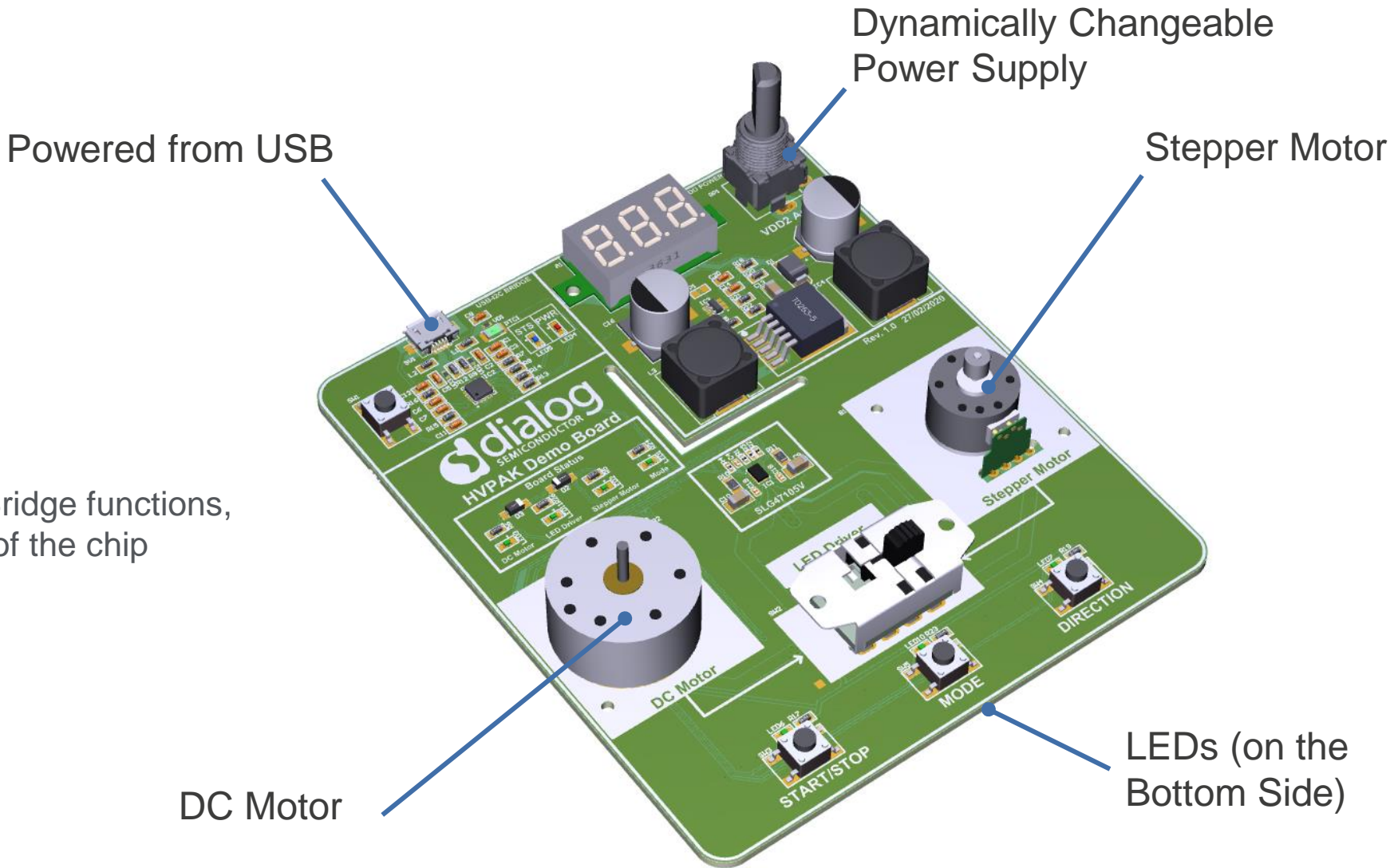


# HVPAK DEMO BOARD

**SLG47105 Demo Board** allows the User to get acquainted with SLG47105's functionality, especially the H-Bridge and Half-Bridge functions, and demonstrates the power part of the chip

[More info](#)

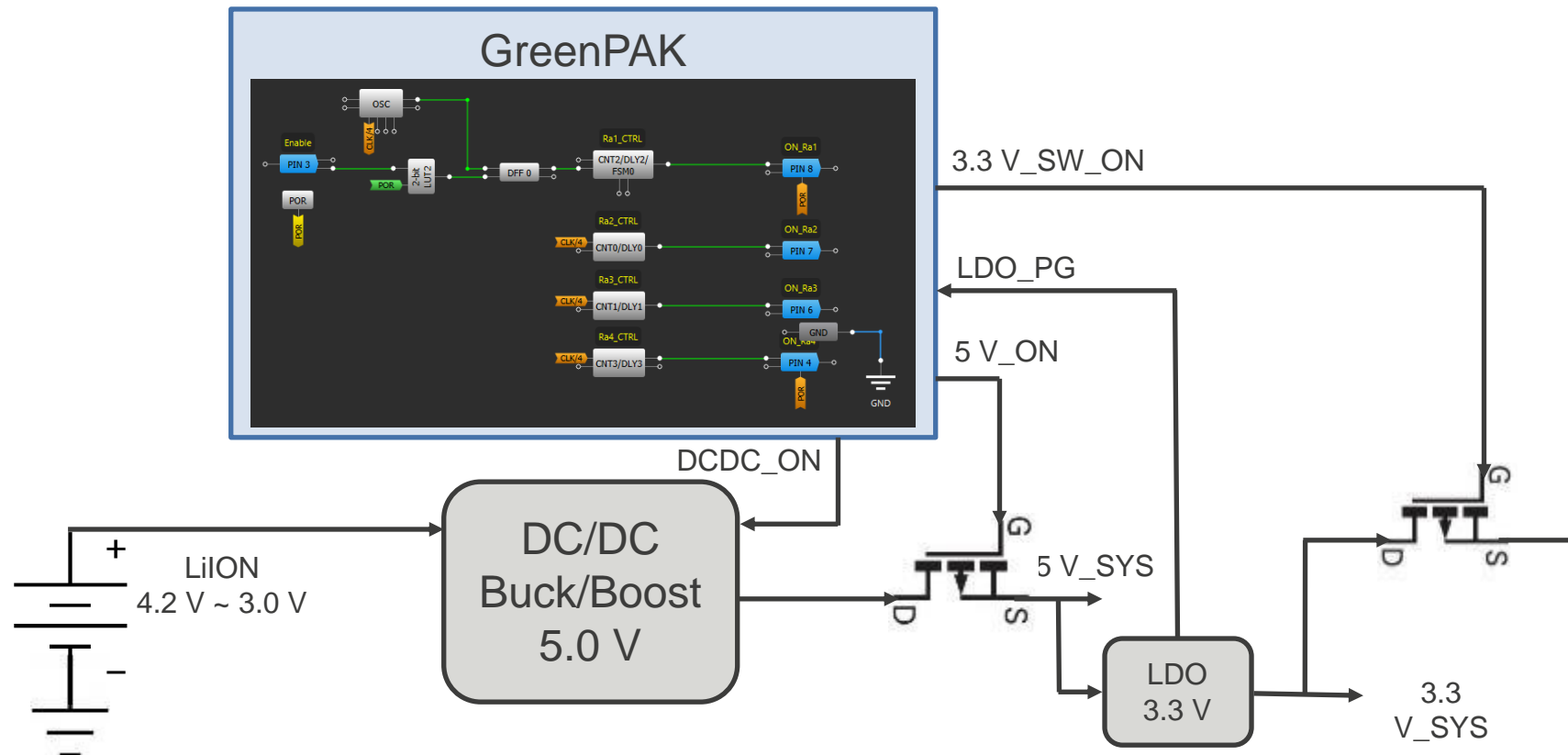
**Demo Board Video**



# GREENPAK APPLICATION EXAMPLES

## Power Rail Sequencing

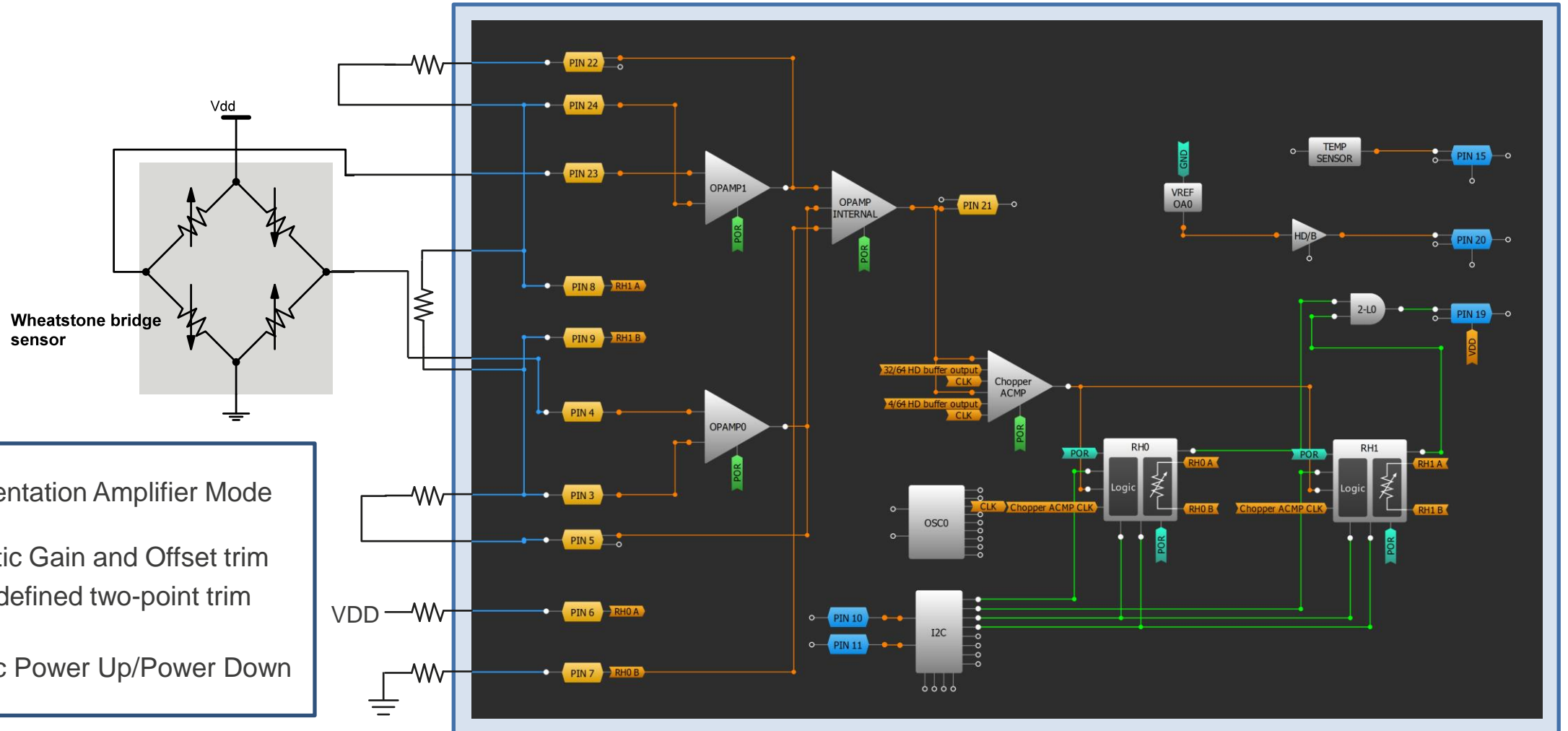
- Can be implemented in any GreenPAK silicon
- Inputs: logic signals, PGs, voltage levels
- Outputs: load switch OEs, LDO OEs, DC/DC OEs, MOSFET gates



# GREENPAK APPLICATION EXAMPLES

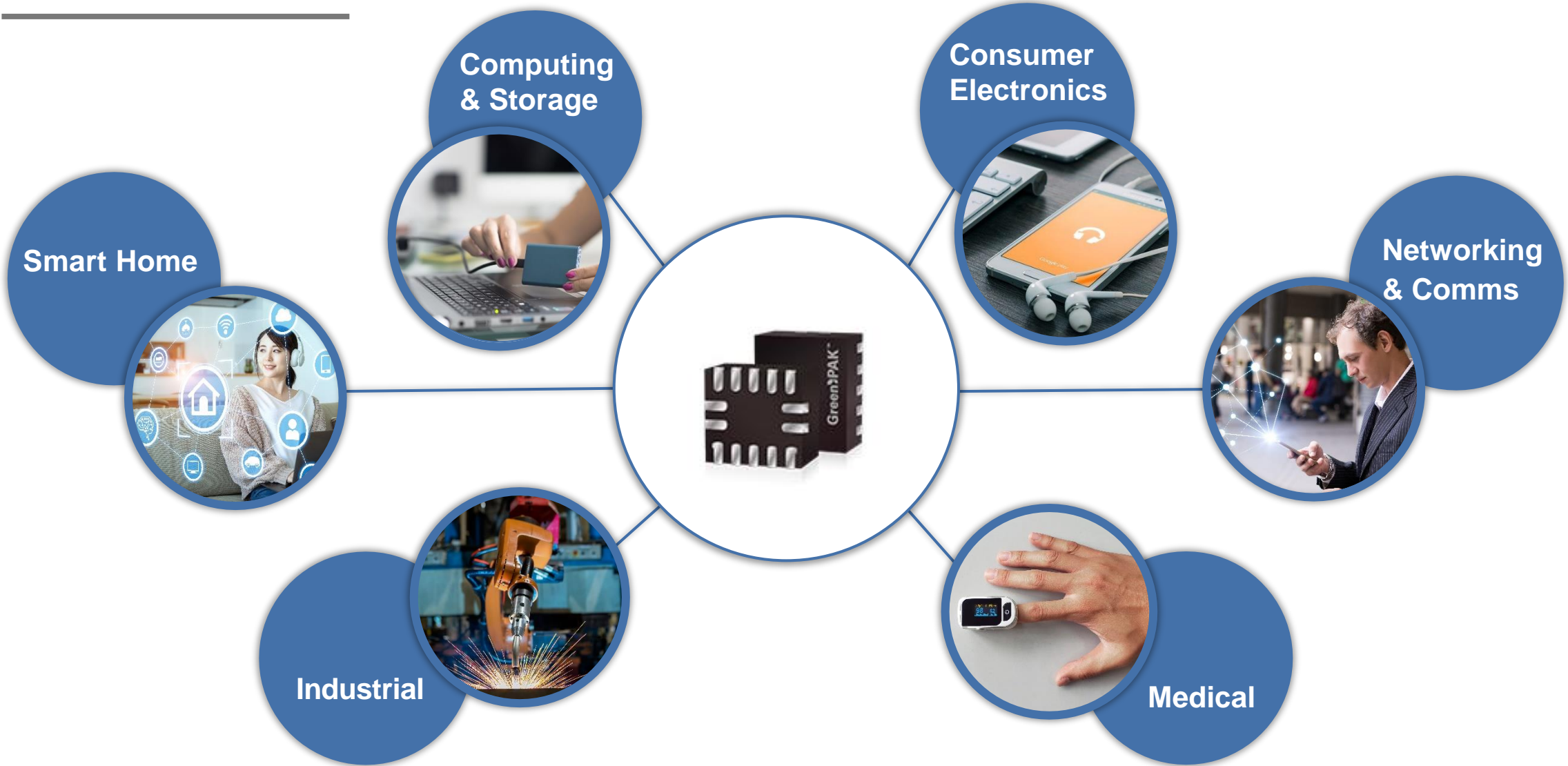
## Wheatstone Bridge Sensors Interface Using AnalogPAK SLG47004

AnalogPAK



- Instrumentation Amplifier Mode
- Automatic Gain and Offset trim or user-defined two-point trim
- Dynamic Power Up/Power Down

# GREENPAK TARGET MARKETS



# GREENPAK IS COST EFFECTIVE

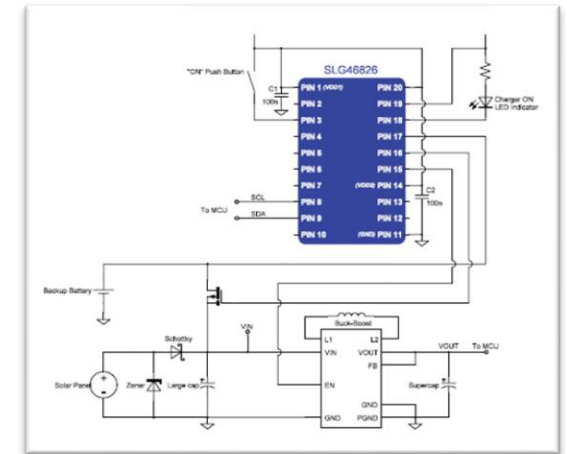
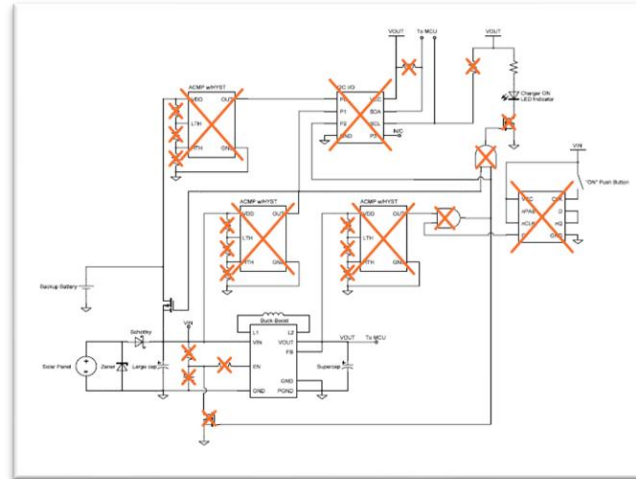
Integrating multiple discrete ICs & passives into GreenPAK lowers design cost

## GreenPAK IC Costs

- Entire portfolio designed to be cost effective
- Fit as much as you can into GreenPAK\*
- Average pricing between **~\$0.10 - \$0.50\*\***
- Auto GreenPAK between **~\$0.35 - \$0.70\*\***

## Other Costs Benefits

- No coding required* – streamlined design time
- Reduced prototyping time
- Reduces need for additional components
- Design changes are quick and inexpensive



Simple or Small Design



More Complex Designs / Higher Integration

\* Cost independent of circuit design

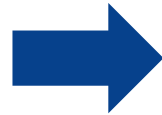
\*\* Volume dependent

# SELECTING RIGHT GREENPAK FOR DESIGN

Best GreenPAK for application dependent on design requirements

## Picking Right Base Die

- Number of GPIO? (6 to 28)
- What is VDD? (1.0V to 5.5V)
- Need for VDD2? (Yes or No)
- SPI or I2C? (Yes, or not required)
- MTP (Multiple-Time Programmable) or OTP?
- Number of voltage rails being monitored?



## What Functions / Features?

- With many use cases for GreenPAK it is important to determine which functions and features would be utilized. Examples Include:

Analog	Digital
■ Analog switch	■ OpAmp
■ Battery charge indicator	■ Over-temp detection
■ Comparators	■ Potentiometer
■ Current sense/limiter	■ Rheostat
■ LDOs	■ Voltage level detection
■ Low voltage indicator	■ Wake/sleep function
■ Logic (Mux, gates, etc.)	■ and More
	■ Control
	■ Deserialization/serialization
	■ Frequency detection
	■ Frequency divider
	■ GPIOs (6-28)
	■ H-/Half-Bridge
	■ I <sup>2</sup> C expansion
	■ Interrupt
	■ LED driving/pattern
	■ Level shifting
	■ Motor driving
	■ Pattern generator
	■ PWM generation
	■ Sequencer
	■ SPI or I <sup>2</sup> C Communication
	■ System reset
	■ Watchdog timer
	■ and More



## Selecting GreenPAK

- Filter by parametric search on web
- Reach out to Distribution FAE /Renesas FAE for support

Simple or Small Design



More Complex Designs / Higher Integration



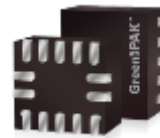
1.0 mm x 1.2 mm  
0.4 mm pitch  
STQFN  
8-pin package



1.6 mm x 1.6 mm  
0.4 mm pitch  
STQFN  
12-pin package



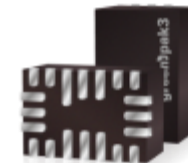
1.6 mm x 2.0 mm  
0.4 mm pitch  
STQFN  
14-pin package



2.0 mm x 2.2 mm  
0.4 mm pitch  
STQFN  
14-pin package



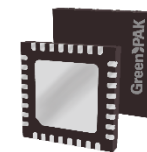
1.6 mm x 2.5 mm  
0.4 mm pitch  
STQFN  
14-pin package



2.0 mm x 3.0 mm  
0.4 mm pitch  
STQFN  
20-pin package



2.0 mm x 2.2 mm  
0.4 mm pitch  
MSTQFN  
22-pin package



4.0 mm x 4.0 mm  
0.4 mm pitch  
STQFN  
32-pin package

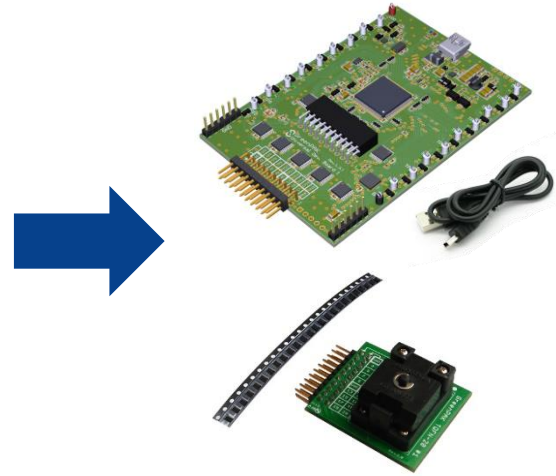
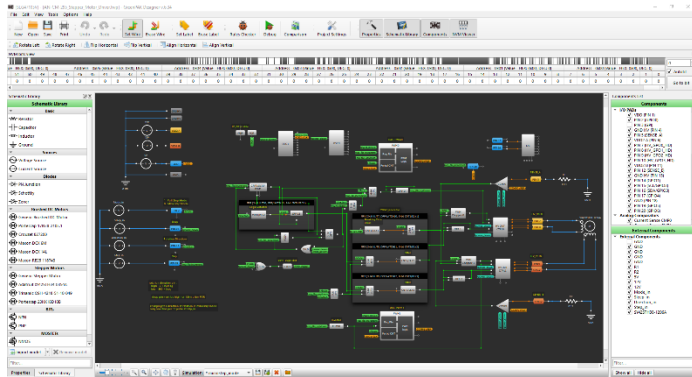
# GREENPAK DESIGN DEVELOPMENT PROCESS

- Development with GreenPAK is **FAST**
- Create a custom design and debug with Evaluation Kit, or program individual ICs at your fingertips



Design Revisions?

Ready for Production Samples?



Production Samples  
Process Covered on Next  
Slide



## GreenPAK Design Created

Design in as little as a few minutes with the [FREE Go Configure Software Hub](#).

## Can Use EVK to Test & Debug\*

Custom design can be tested with EVK or **FREE** samples requested from Renesas

## Program at Your Desk

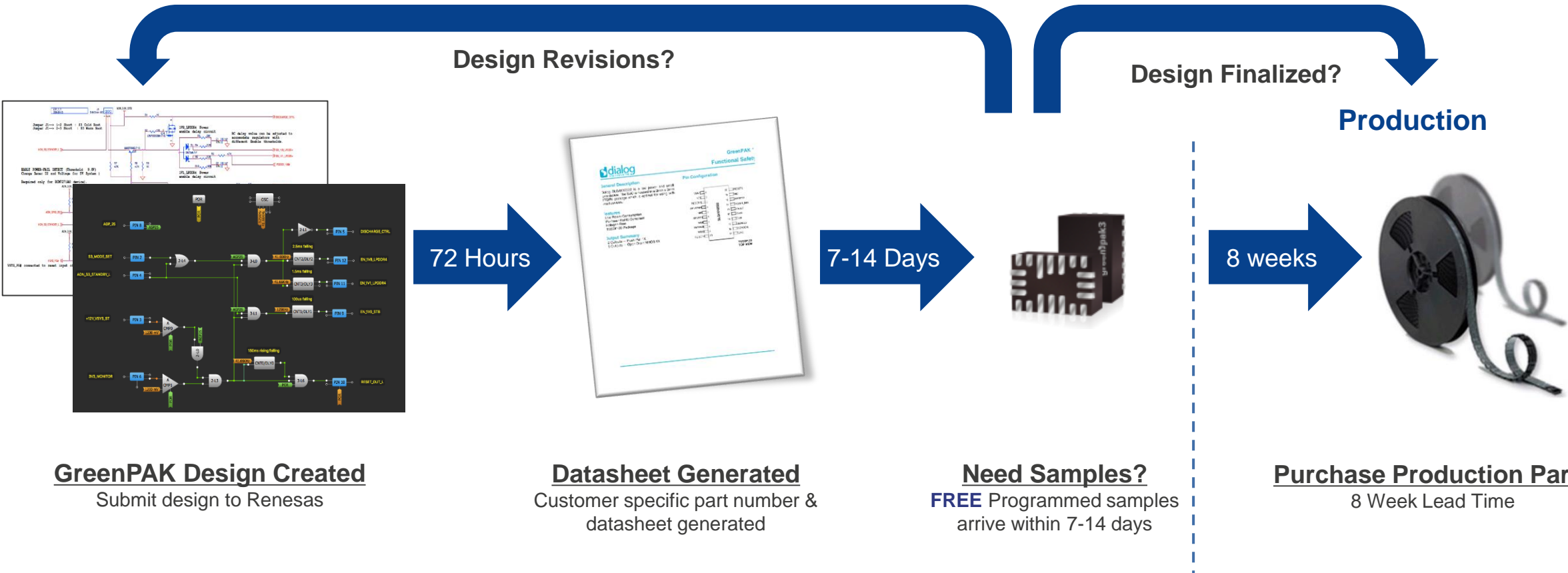
Can program prototype ICs at your fingertips or ask Renesas for **FREE** programmed samples

Circuit design is done via SW

**No EVK needed for creation of design!**

# GREENPAK SAMPLE & PRODUCTION FLOW

- Design changes can be made throughout the development cycle
- Datasheet revision and part top markings reflect different versions of the device through development



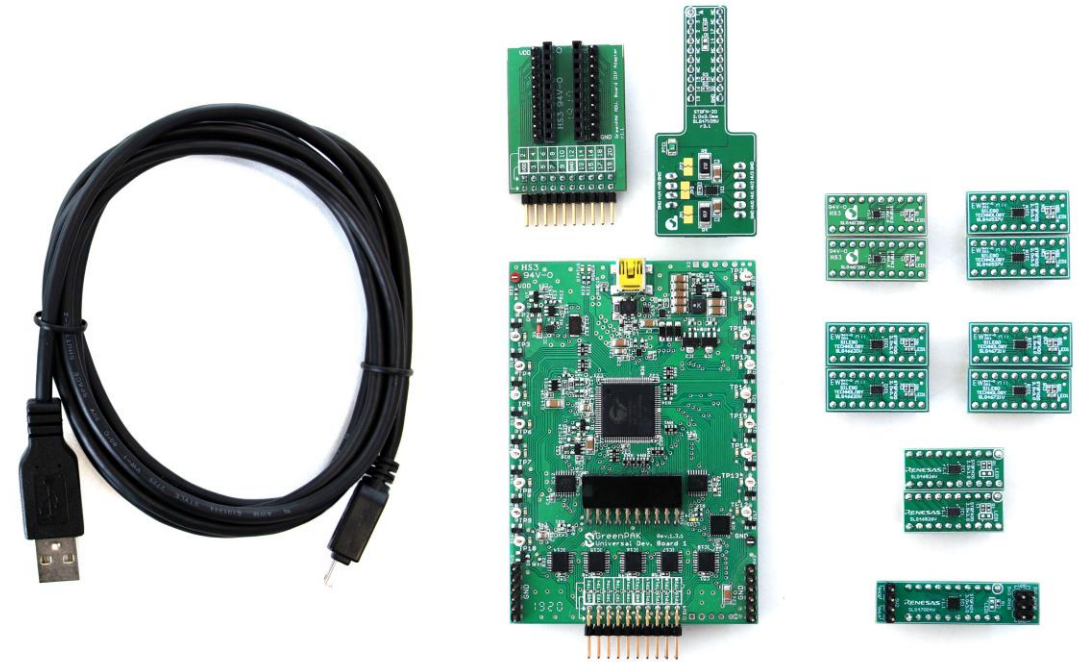


# GREENPAK DEVELOPMENT BOARDS

# GREENPAK DEVELOPMENT TOOLS – STARTING WITH HARDWARE

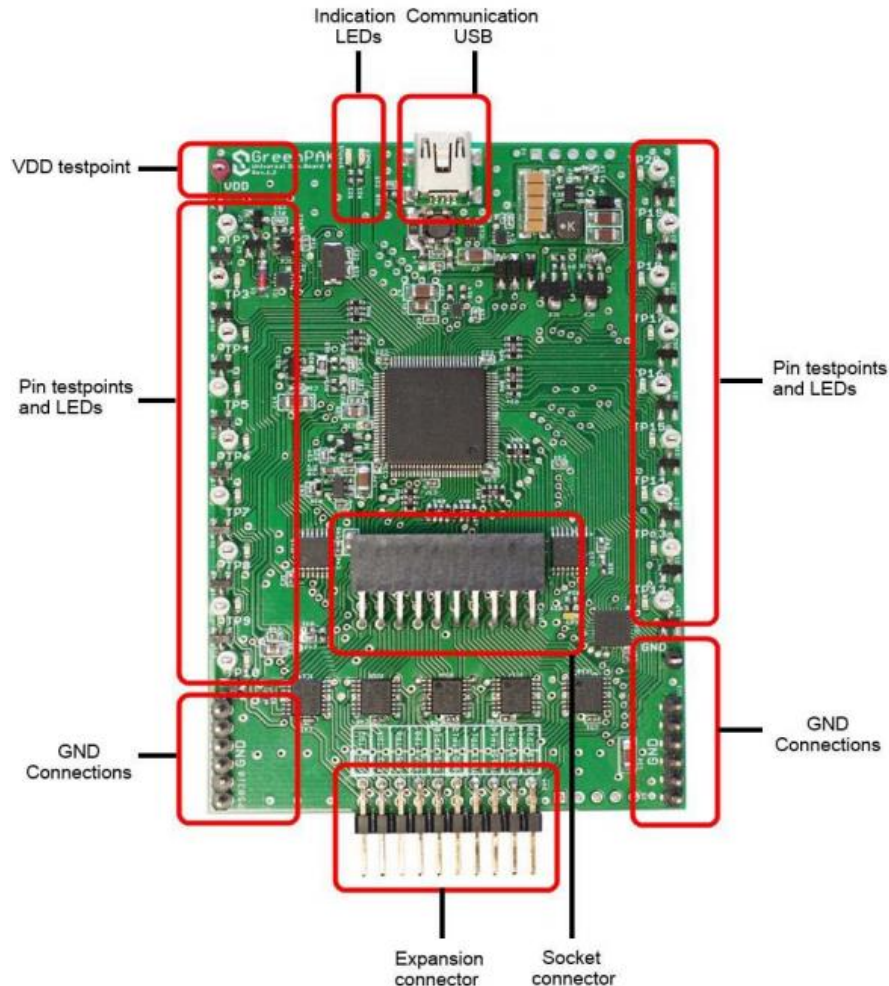
## Where to start with hardware:

- If hardware is required Renesas FAE or GreenPAK product line can provide feedback on which tools / devices to begin design with
- Another option is the [SLG4DVKINTRO – GreenPAK Introduction Kit](#) which includes:
  - 1x Universal Development Board (this might later change to the Lite board, but for now it is Advanced Dev Board)
  - 1x USB cable
  - 1x SLG4SADIP
  - 2x SLG46120V-DIP
  - 2x SLG46721V-DIP
  - 2x SLG46620V-DIP
  - 2x SLG46537V-DIP
  - 2x SLG46826V-DIP
  - 1x SLG47105V-DIP
  - 1x SLG47004V-DIP



# GREENPAK DEVELOPMENT HARDWARE

## Advanced Development Platform






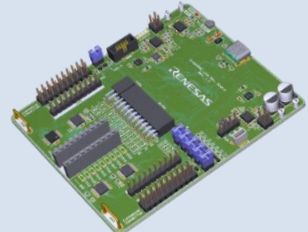




## Provides Full Programming, Emulation and Testing Functionality:

- On Board Signal and Logic Generators
- Socket Connection for GreenPAK Socket Adapters
- USB Mini-b Connector for GreenPAK Software Designer Interface
- LEDs and Test Points for each GPIO
- Expansion Connector for Signal Injection



# GREENPAK DEVELOPMENT HARDWARE

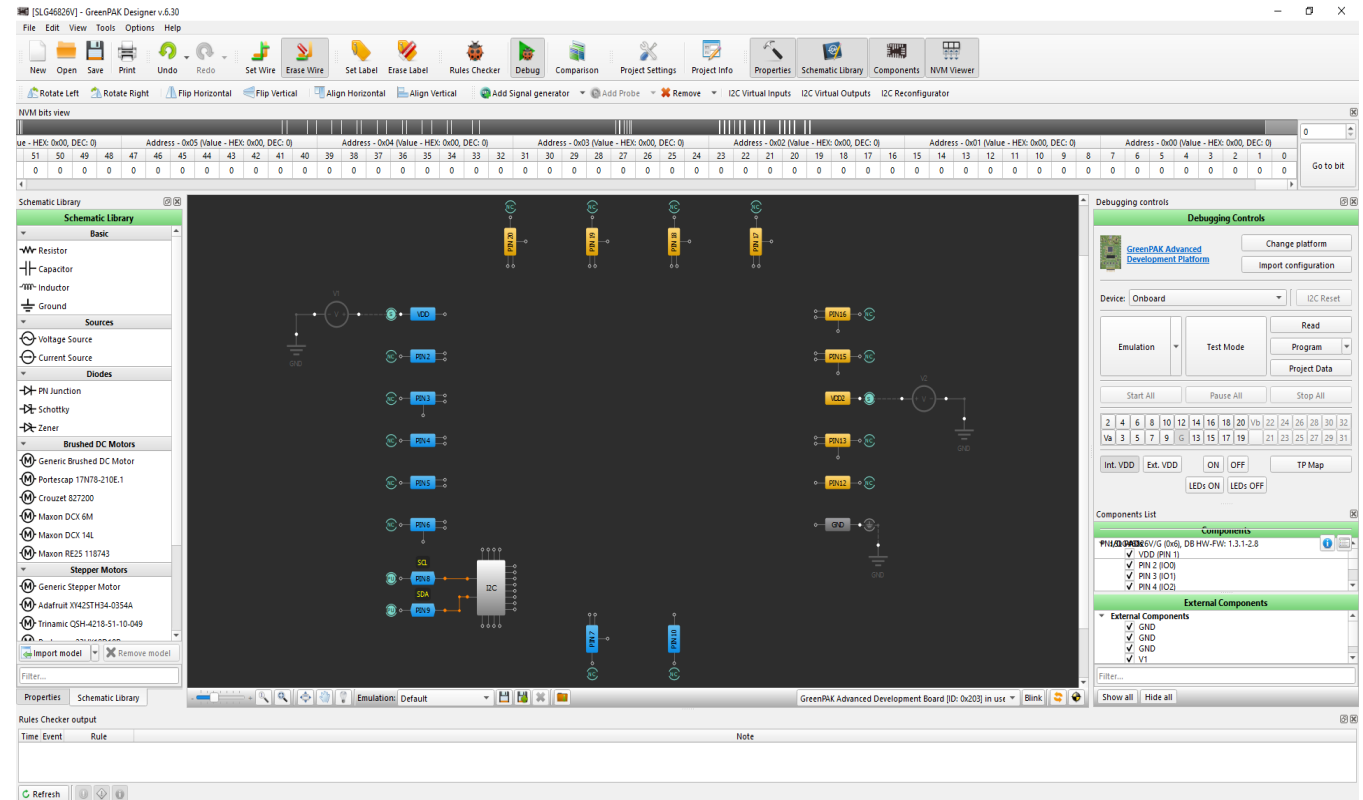
Board/Functions	Features		
<p><b>GreenPAK Advanced Development Platform</b> Program custom samples in minutes using any GreenPAK device.</p>	<ul style="list-style-type: none"> <li>▪ USB interface</li> <li>▪ MacOS, Windows and Linux compatible</li> <li>▪ Programming and Emulation</li> <li>▪ Gated expansion header for connection to external test equipment</li> <li>▪ Integrated signal and logic generators</li> <li>▪ LEDs and Test Points for each GPIO</li> </ul>		
<p><b>GreenPAK Serial Debugger Board (GSD)</b> Serial debugging for all GreenPAK parts with I<sup>2</sup>C.</p>	<ul style="list-style-type: none"> <li>▪ USB interface for power and control</li> <li>▪ 4 pin header with I<sup>2</sup>C interface to target system</li> <li>▪ MacOS, Windows and Linux compatible</li> <li>▪ GSD supports serial programming for SLG46827</li> </ul>		
<p><b>GreenPAK Development Board Lite</b> Supports Programming and Emulation for Breadboarding and Fast Prototyping</p>	<ul style="list-style-type: none"> <li>▪ USB interface</li> <li>▪ MacOS, Windows and Linux compatible</li> <li>▪ Gated expansion header for connection to external test equipment</li> <li>▪ LEDs for visual indication</li> <li>▪ Real-time power monitor function</li> </ul>		
<p><b>GreenPAK DIP Development Platform</b> Perfect for breadboarding and fast prototypes</p>	<ul style="list-style-type: none"> <li>▪ USB interface</li> <li>▪ MacOS, Windows and Linux compatible</li> <li>▪ Programming and Emulation</li> <li>▪ Gated expansion header for connection to external test equipment</li> </ul>		

Available online from local/global distribution partners!

# GREENPAK DEVELOPMENT SOFTWARE

# GREENPAK SOFTWARE

- Create custom solutions, simulate circuit
- Debug, program ICs,
- EVK hardware is **NOT** needed to get started



# GREENPAK DEVELOPMENT SOFTWARE

## Go Configure Software Hub

The screenshot displays the GreenPAK Designer software interface. At the top, the 'Part Family' is set to 'AI' and the selected part is 'SLG46826V'. Below this is a table listing various GreenPAK ICs with columns for Part Number, DS, VDD (V), VDD2 (V), GPIO, AEC-Q100, Special Features, ACHP, DCMP, Max. CNT/DLY, Max. LUT, and Max. DFF. The 'Details' pane for the selected SLG46826V part is visible, showing package information (STQFN-20), supported development platforms, and a detailed description of the device's capabilities and features.

Part Number	DS	VDD (V)	VDD2 (V)	GPIO	AEC-Q100	Special Features	ACHP	DCMP	Max. CNT/DLY	Max. LUT	Max. DFF
SLG51000C	<a href="#">Contact us</a>	2.8 to 5.0	-	6	-	-	-	-	-	12	-
SLG51001C	<a href="#">Contact us</a>	2.8 to 5.0	-	4	-	-	-	-	-	12	-
SLG47910V	<a href="#">Contact us</a>	0.99 to 1.21	1.71 to 3.6	19 + PWR, EN	-	Dense Logic Array; PLL; BRAM	-	-	-	-	-
SLG51002C	<a href="#">Contact us</a>	2.8 to 5.0	1.2 to 5.0	6	-	-	-	-	-	8	-
SLG47004V	<a href="#">PDF</a>	2.4 to 5.5	-	8	-	-	-	-	-	7	20
SLG47115V	<a href="#">Contact us</a>	2.3 to 5.5	4.5 to 26.4	8 + 2x HD	-	2x Op Amp or 1x In-Amp; 2x Rheostat; 2x An Switch; 2-Ch Auto-Trim; EEPROM	3	-	-	5	17
SLG47105V	<a href="#">PDF</a>	2.3 to 5.5	3.0 to 13.2	8 + 4x HD	-	1x H/2x Half-Bridge; 2x PWM; COMP; Int&Dff Amp	2	-	-	5	17
SLG46811V	<a href="#">PDF</a>	2.3 to 5.5	-	10	-	2x H/4x Half-Bridge; 2x PWM; 2x COMP; Int&Dff Amp	2	-	-	5	17
SLG47513M	<a href="#">PDF</a>	1.0 to 1.65	-	14	-	92 x 8 bit Pattern Generator	1 (4)	-	-	6	18
SLG47512V	<a href="#">PDF</a>	1.0 to 1.65	-	10	-	-	2	-	-	8	23
SLG46867M	<a href="#">PDF</a>	2.3 to 5.5	-	10	-	2x P-FET (44mΩ, 2A)	4	-	-	8	23
SLG46857-AP	<a href="#">Contact us</a>	2.3 to 5.5	-	12	Grade 1	-	4	-	-	8	23
SLG46855-AP	<a href="#">Contact us</a>	2.3 to 5.5	-	12	Grade 2	-	4	-	-	8	23
SLG46855V	<a href="#">PDF</a>	2.3 to 5.5	-	12	-	-	4	-	-	8	23
SLG46827-AG	<a href="#">PDF</a>	2.3 to 5.5	1.71 to VDD	17	Grade 2	-	4	-	-	8	19
SLG46826G	<a href="#">PDF</a>	2.3 to 5.5	1.71 to VDD	17	-	-	4	-	-	8	19
SLG46826V	<a href="#">PDF</a>	2.3 to 5.5	1.71 to VDD	17	-	-	4	-	-	8	19

## Tabs

- Welcome: Design Tips, Links to Product Brochures, Application Notes, and Training Videos
- Develop: Table of GreenPAK ICs with their PCB Footprint and Logic Resource Availability
- Demo: List of Common GreenPAK Applications
- Datasheets
- User Guides

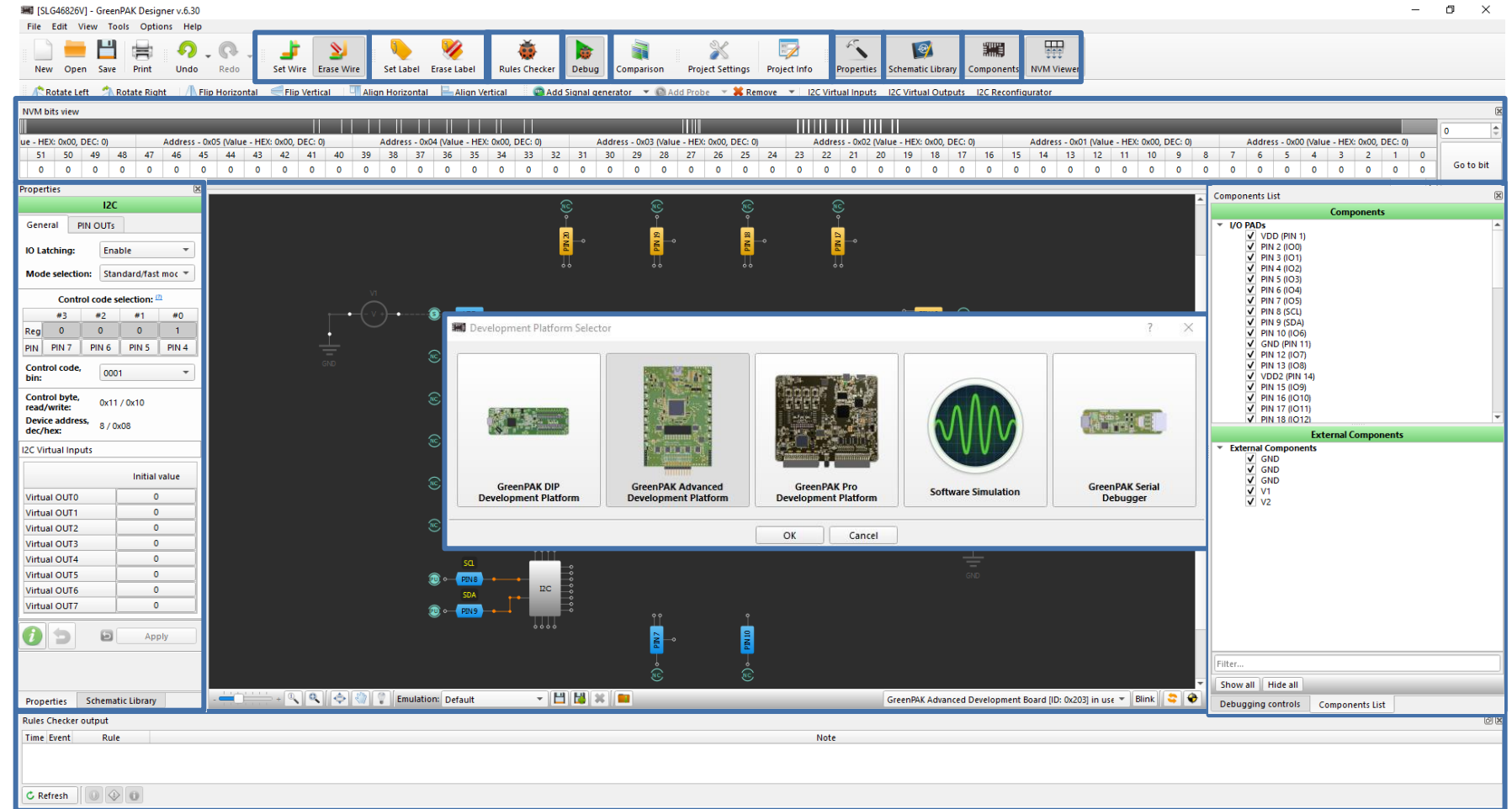
[Go Configure Software Hub - GreenPAK Designer | Renesas](#)

# GREENPAK DEVELOPMENT SOFTWARE

## GreenPAK Designer

### Tool Bar

- Set / Erase Wire
- Set / Erase Label
- Rules Checker
- Debug
- Project Settings
- Project Info
- Properties
- Schematic Library
- Components
- NVM Viewer
- Change platform





# GREENPAK DEVELOPMENT SOFTWARE

## GreenPAK Designer

### Software Simulation

- Voltage Source
- Add Probe
- Remove
- Debugging Controls

The screenshot displays the GreenPAK Designer v.6.30 software interface. The main window shows a schematic diagram with a voltage source (V3) and two probes (V1 and V2). A 'Source Setup' dialog box is open, showing the 'General' tab with 'Source: V3', 'Name: V3', and 'Pre-start delay: 0.000 ms'. The 'Voltage Source Settings' dropdown menu is open, showing options like DC, Trapezoid, Sine, Exponential, Custom signal, Logic pattern, and Clock generator. The 'Sine' option is selected. The 'Debugging Controls' panel is also visible, showing 'Software Simulation' and 'Transient' analysis type. The 'Start simulation' button is highlighted. The 'Components List' panel shows 'I/O PADS' and 'External Components'.

Source Setup

Options

General

Source: V3

Name: V3

Pre-start delay: 0.000 ms

Show only one period

Limit voltage to VDD and GND level

Customize source

Internal capacitance: 10.000 pF

Internal resistance: 10.000 Ohms

Copy from: Copy

Voltage Source Settings

Transi: DC, Trapezoid, Sine, Exponential, Custom signal, Logic pattern, Clock generator

Type: Sine

Zero o

Amplit

Frequency: Hz

Damping factor: 0.000 Hz

Apply

Debugging controls

Debugging Controls

Software Simulation

Change platform

Import configuration

Analysis Type: Transient

Transient analysis settings:

Ending time: 12ms

Maximum time step: 20us

Temperature: 25.00°C

Use initial conditions

Estimated completion time is less than 30 seconds

Start simulation

Show plots

Components List

Components

I/O PADS

✓ VDD (PIN 1)

✓ PIN 2 (IO0)

✓ PIN 3 (IO1)

✓ PIN 4 (IO2)

External Components

✓ GND

✓ GND

✓ GND

✓ V1

Filter...

Show all Hide all

# GREENPAK DEVELOPMENT SOFTWARE

## GreenPAK Designer

### Debug with Hardware

- Logic generator
- Signal generator
- I2C generator

The screenshot displays the GreenPAK Designer v.6.30 software interface. The main window shows a timing diagram with three traces: PIN3 (TP3), PIN4 (TP4), and PIN4 (TP4). The Signal Wizard dialog is open, showing the following settings:

- General:** Generator: PIN3 (TP3) - Logic Sequence; Shown period: Auto; Start point: 0.000 ms; Stop point: 100.000 ms; Global linkage: Linked; Sync Power Rails: Disabled; Repeat: Cyclic; Repeat count: 2; Pre-start state: Low; Pre-start delay: 0.000 ms; End state: Pre-start state; Output type: Push-Pull; Pause type: Last state.
- Logic Generator Settings:** Mode: Normal; Pattern: 101.

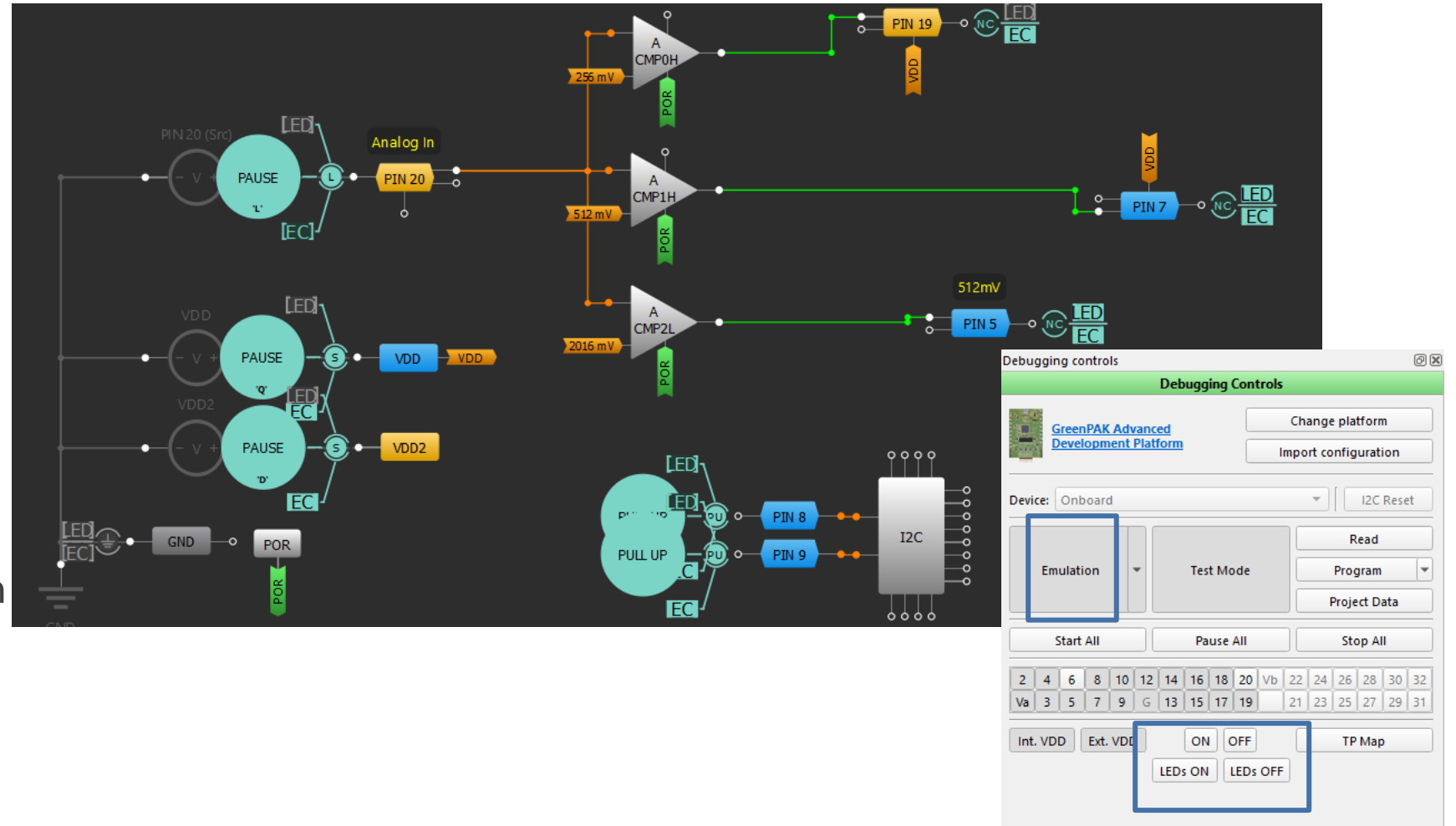
The timing diagram shows three traces: PIN3 (TP3), PIN4 (TP4), and PIN4 (TP4). The PIN3 (TP3) trace shows a square wave pulse. The PIN4 (TP4) traces show a square wave pulse. The Debugging Controls panel is visible on the right, showing the device as Onboard and various debugging options.

# GREENPAK DEVELOPMENT SOFTWARE

## GreenPAK Designer

### Emulation Mode together with Evaluation Boards

- Add Logic Generator
- Add I2C Generator
- Add Signal generator
- **Debug with Hardware**
- Test your Greenpak Programming on Evaluation Board
- LEDs at Test Points can be turned ON /OFF for better debugging



# GREENPAK FOR LED CONTROL

# WHY IS GREENPAK GOOD FOR LED CONTROL APPLICATIONS?

---

- High drive strength I/Os on GreenPAK allow for direct LED drive
- Multiple output modes allow for your choice in LED drive
- LED dimming and LED breathing can be implemented without any processor overhead
- Can use I<sup>2</sup>C to remotely control LEDs – very easy to implement
- You can customize any way you want

# DESIGN DEMONSTRATION #1

---

- Usage of AMPs to create three different control pins for an RGB-LED
- Goal to switch LEDs when input voltage is higher than ACMP's threshold
- ACMP has different references applied to IN-
- By increasing the voltage at PIN20, the outputs will go HIGH

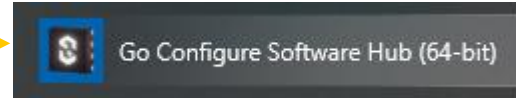
# STARTING THE PROCESS

## Launch GreenPAK Designer

- After you have installed [GoConfigure Software Hub](#), open up the program
- Click the Windows button in the bottom left corner of your screen
- Scroll to the GoConfigure Software Hub icon and click once to open it
- Click the GoConfigure Software Hub

- The first time you launch GoConfigure Software Hub, you will land on the Welcome page. Click the “Develop” page next.

- This will give you a window that shows the selection of GreenPAK parts available
- Single click the SLG46826V to highlight it
- Double click on SLG46826V to launch the designer for this silicon



The screenshot shows the GoConfigure Software Hub interface. The 'Develop' tab is active, displaying a table of GreenPAK parts. The SLG46826V part is highlighted in blue. The table includes columns for Part Number, DS, VDD (V), VDD2 (V), GPIO, AEC-Q100, Special Features, ACPM, DCMP, Max. CNT/DLY, Max. LUT, and Max. DFF.

Part Number	DS	VDD (V)	VDD2 (V)	GPIO	AEC-Q100	Special Features	ACPM	DCMP	Max. CNT/DLY	Max. LUT	Max. DFF
SLG51000C	Contact us	2.8 to 5.0	-	6	-	-	-	-	-	12	-
SLG31001C	Contact us	2.8 to 5.0	-	4	-	-	-	-	-	12	-
SLG47910V	Contact us	0.99 to 1.21	1.71 to 3.6	19 + PWR, EN	-	Dense Logic Array; PLL; BRAM	-	-	-	-	-
SLG51002C	Contact us	2.8 to 5.0	1.2 to 5.0	8	-	-	-	-	-	8	-
SLG47004V	PDF	2.4 to 5.5	-	8	-	2x Op Amp or 1x In-Amp; 2x Rheostat; 2x An. Switch; 2-Ch Auto-Trim; EEPROM	3	-	7	20	1
SLG47115V	PDF	2.3 to 5.5	4.5 to 26.4	8 + 2x HD	-	1x H/2x Half-Bridge; 2x PWM; COMP; IntSDIO Amp	2	-	5	17	1
SLG47105V	PDF	2.3 to 5.5	3.0 to 13.2	8 + 4x HD	-	2x H/4x Half-Bridge; 2x PWM; 2x COMP; IntSDIO Amp	2	-	5	17	1
SLG46811V	PDF	2.3 to 5.5	-	10	-	92 x 8 bit Pattern Generator	1 (4)	-	6	18	1
SLG47513M	PDF	1.0 to 1.65	-	14	-	-	2	-	8	23	2
SLG47512V	PDF	1.0 to 1.65	-	10	-	-	2	-	8	23	2
SLG46826V	PDF	2.3 to 5.5	-	10	-	2x P-FET (44mΩ, 2A)	4	-	8	23	2
SLG46857-AP	Contact us	2.3 to 5.5	-	12	Grade 1	-	4	-	8	23	2
SLG46855-AP	Contact us	2.3 to 5.5	-	12	Grade 2	-	4	-	8	23	2
SLG46855V	PDF	2.3 to 5.5	-	12	-	-	4	-	8	23	2
SLG46827-AG	PDF	2.3 to 5.5	1.71 to VDD	17	Grade 2	-	4	-	8	19	1
SLG46836G	PDF	2.3 to 5.5	1.71 to VDD	17	-	-	4	-	8	19	1
SLG46826V	PDF	2.3 to 5.5	1.71 to VDD	17	-	-	4	-	8	19	1

Details for SLG46826V:

- Package: STQFN-20
- Supported Development Platforms:
  - Software Simulation
  - GreenPAK Serial Debugger (SLG4DV02SD)
  - GreenPAK DFP Development Board (SLG4DV02DP) + 2x DFP Proto Board (SLG46826V-DFP)
  - GreenPAK Advanced Development Board (SLG4DV02AD) + Training Adapter #1 (SLG4TA205P-SLG46826), is optional + TQFN-20 #4 (SLG4SA205P-20x30)
  - GreenPAK Pro Development Board (SLG4DV02P) + TQFN-20 #4 (SLG4SA205P-20x30)
- Descriptions:
  - The SLG46826V/G provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the multiple time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O pins and the macrosells of the SLG46826V/G. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrosells in the device include the following:
    - Two High Speed General Purpose Rail-to-Rail ACPMs;
    - Two Low Power General Purpose Rail-to-Rail ACPMs;
    - Two Voltage References (Vref);
    - Two Vref Outputs;
    - Eleven Combination Function Macrosells:
      - Three Selectable DFF/Latch or 2-bit LUTs;
      - One Selectable Programmable Pattern Generator or 2-bit LUT;
      - 5x Selectable DFF/Latch or 3-bit LUTs;
      - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT;
    - Eight Multi-Function Macrosells:
      - Seven Selectable DFF/Latch or 3-bit LUTs + 8-bit Delay/Counter;
      - One Selectable DFF/Latch or 4-bit LUT + 16-bit Delay/Counter;
    - Serial Communications:
      - IC Protocol Interface;
    - 2-Kbit (256 x 8) I2C-Compatible (2-Wire) Serial EEPROM emulation with Software Write Protection;
    - Programmable Delay with Edge Detector Outputs;
    - Additional Logic Function – 1 Output Filter with Edge Detector;
    - Three On-chip MFCs.

# SETTING UP PROJECT INFO

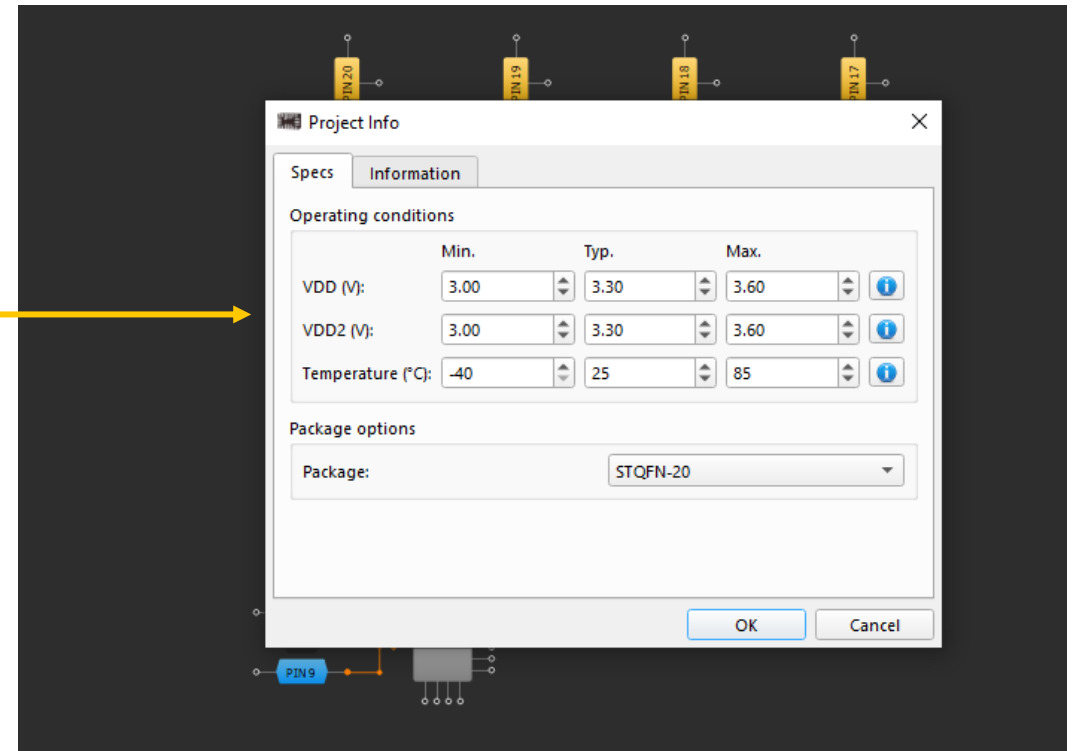
## Entering VDD, VDD2 and Temperature Information

- You will get a window with “Project Info” that opens automatically

- Set:

- VDD to 3.0, 3.3, 3.6
- VDD2 to 3.0, 3.3, 3.6
- Temp to -40, 25, 85

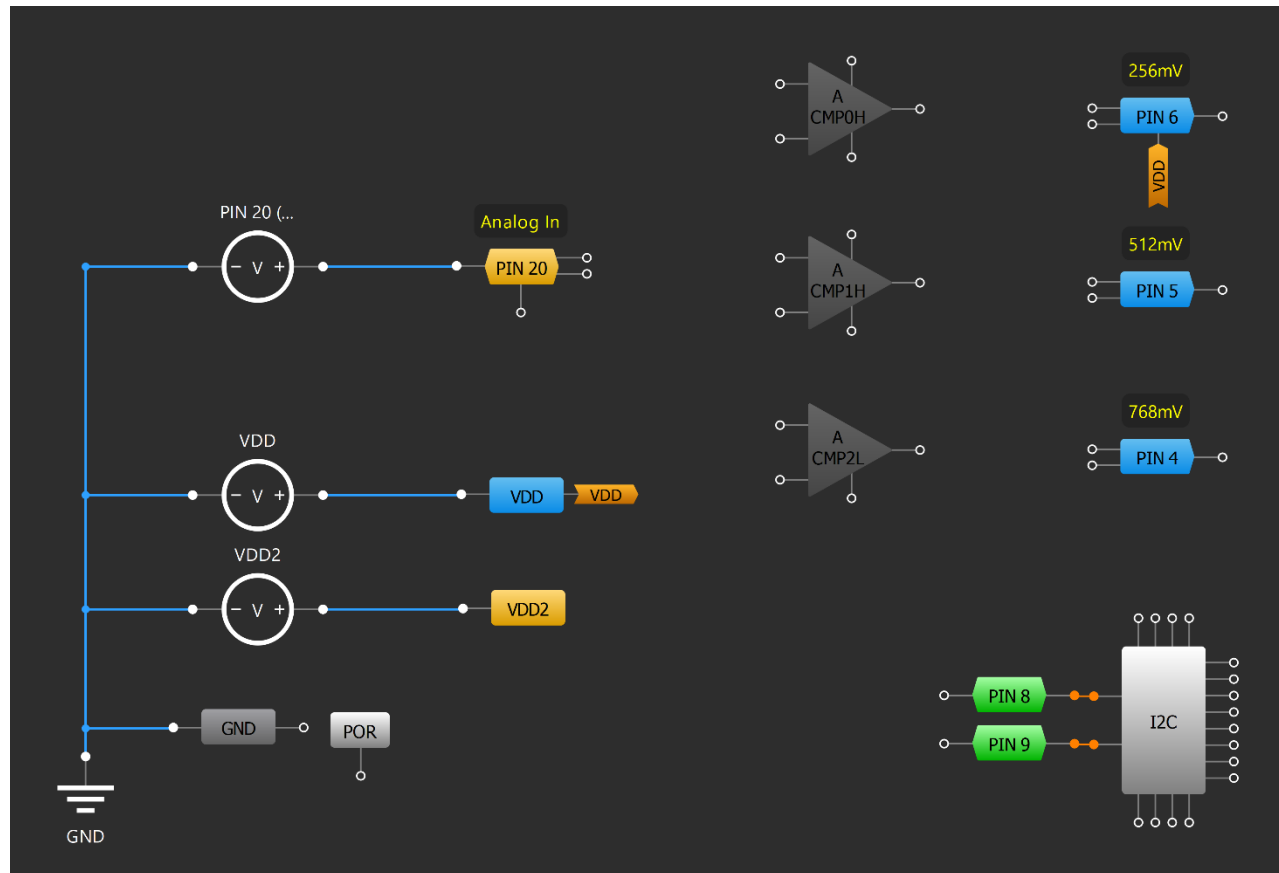
- This information will be used when we want to test or simulate the design





# DESIGN DEMONSTRATION #1

## Usage of AMPs to create three different control levels for an RGB-LED



Design\_Demonstration\_2.gp6

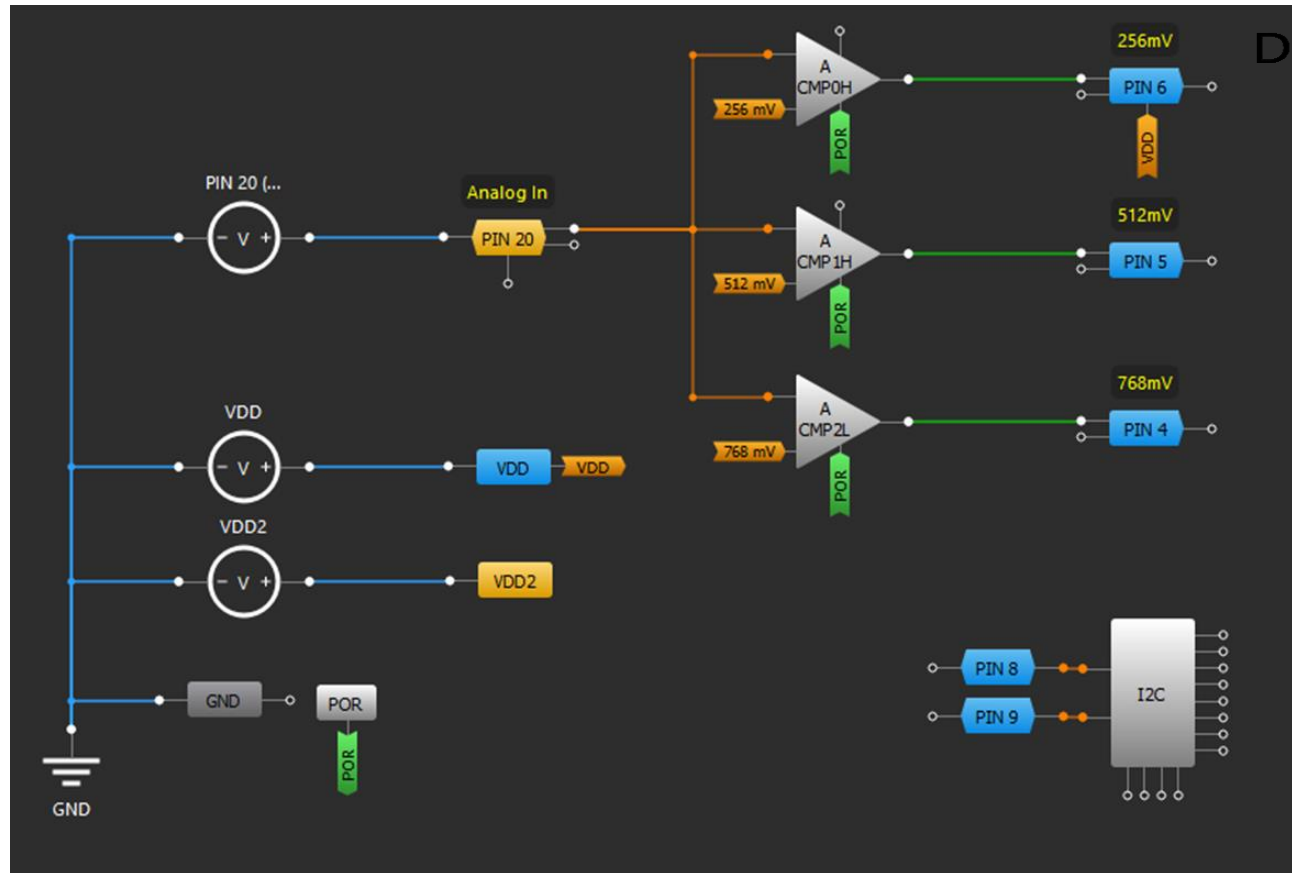
- Goal to switch LEDs when input voltage is higher than ACMP's threshold
- ACMP has different references applied to IN-
- By increasing the voltage at PIN20, the outputs will go HIGH

# DESIGN DEMONSTRATION #1

Usage of AMPs to create three different control levels for an RGB-LED



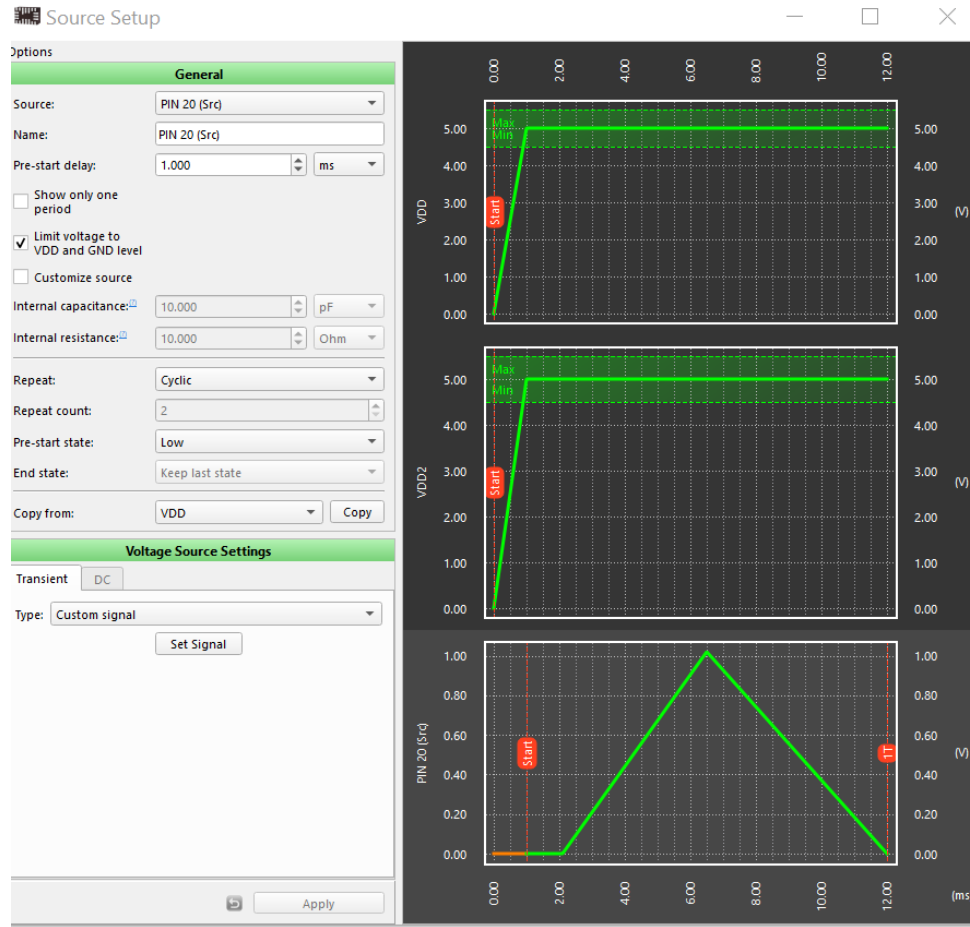
Design\_Demonstration\_2\_finished.gp



- Power Up the ACMP by connecting POR to PWR UP input
- Change the reference in each ACMP to the given value

# DESIGN DEMONSTRATION #1: SIMULATION SETUP

## Voltage source setup

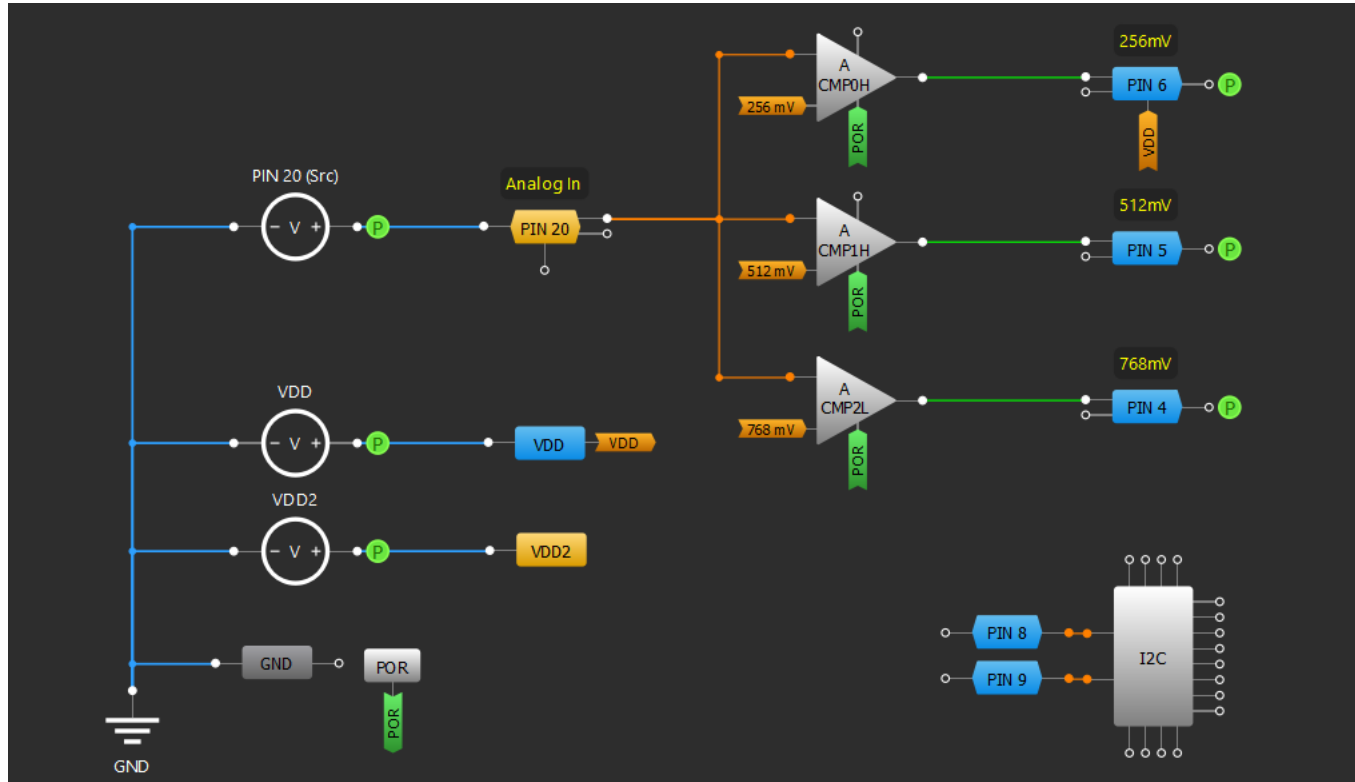


- $VDD = VDD2 = 5V$
- $V(\text{Pin } 20) = \text{triangle}$



# DESIGN DEMONSTRATION #1: ADDING PROBES FOR TESTING

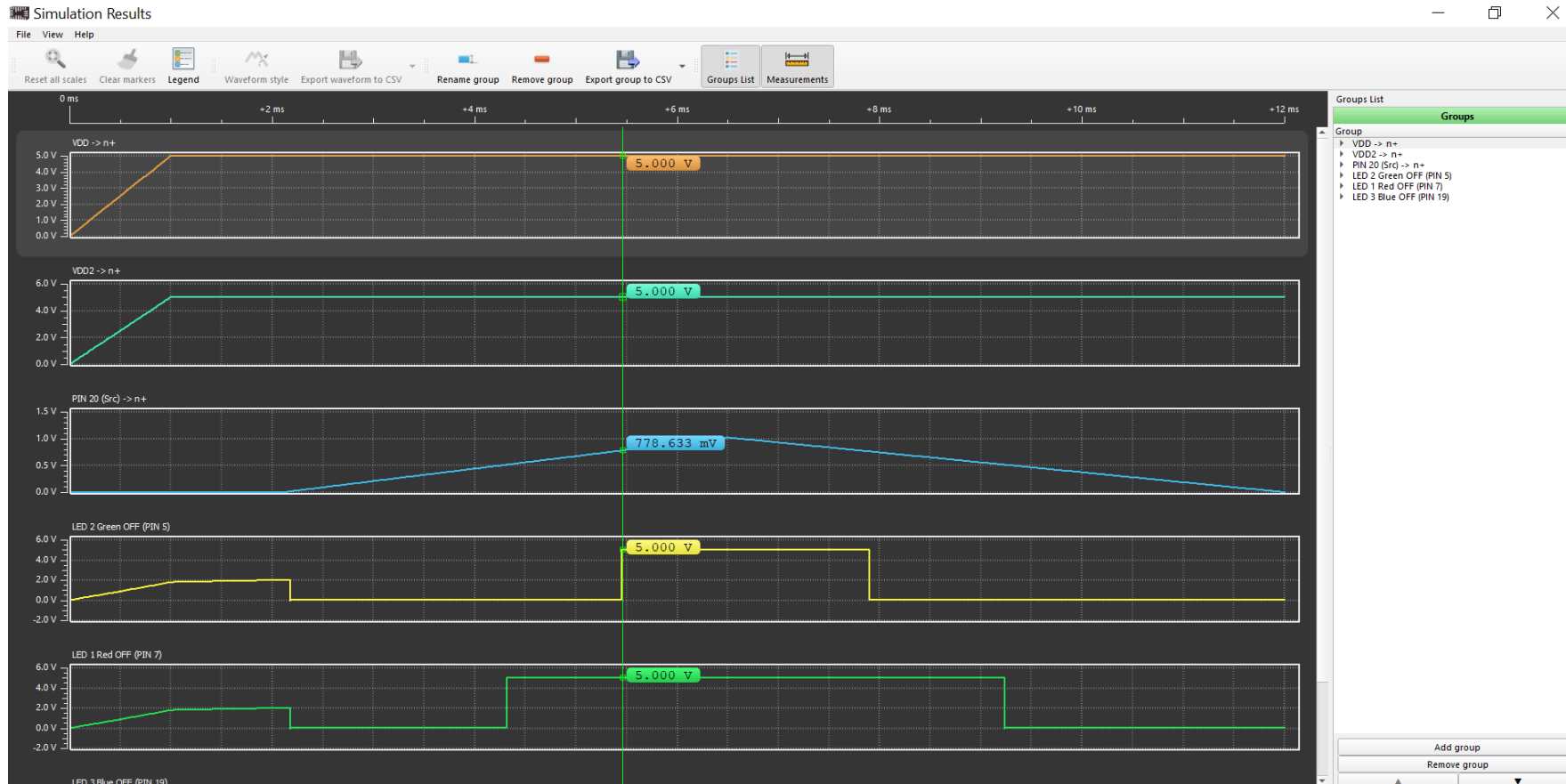
## Add probes



- Add probes where you want to see waveforms
- Parametric probes allow you to see counter states (can right-click on probe symbol to add)

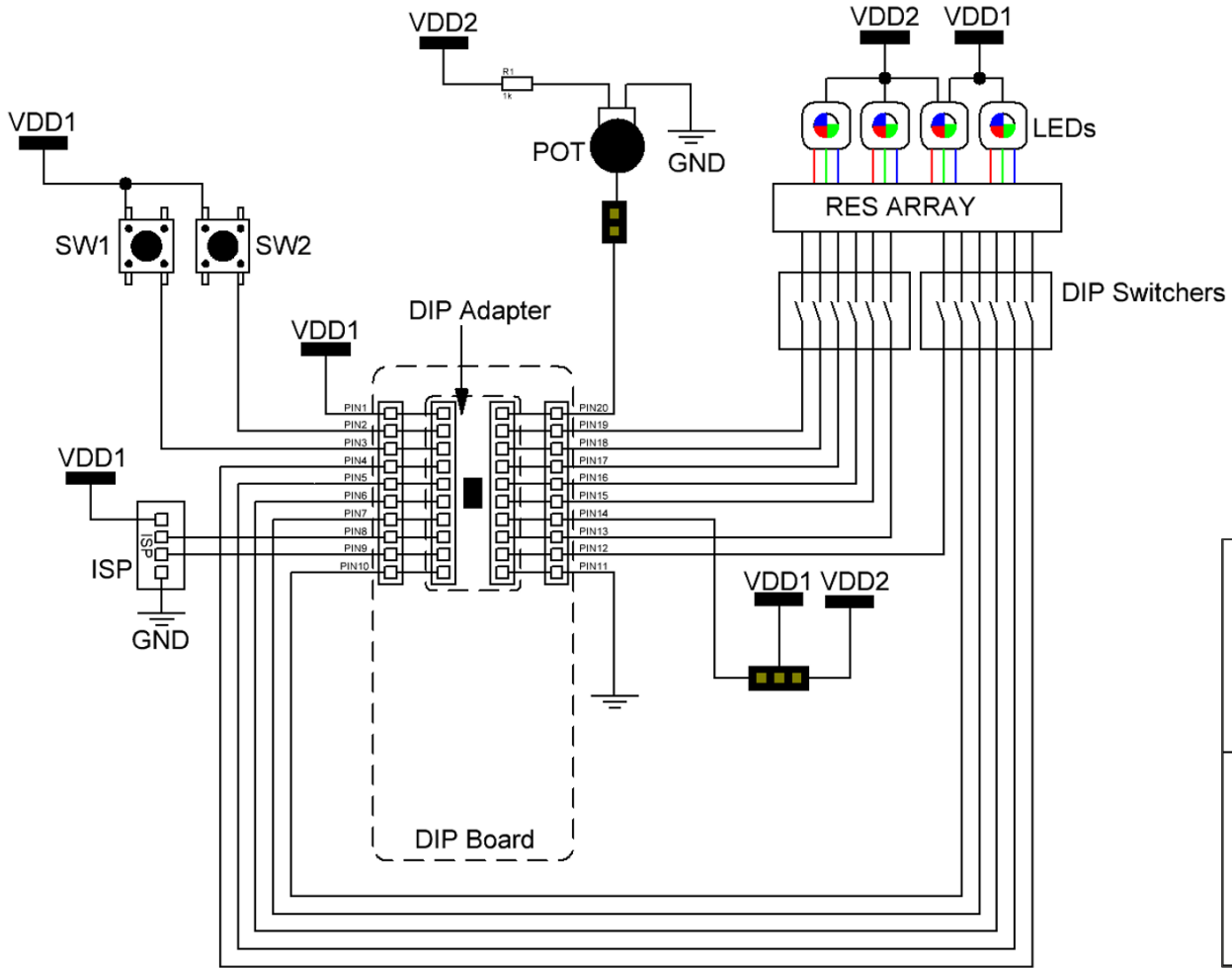
# DESIGN DEMONSTRATION #1: SPICE SIMULATION

## ACMPs and Spice Simulation



- Read out values with Markers

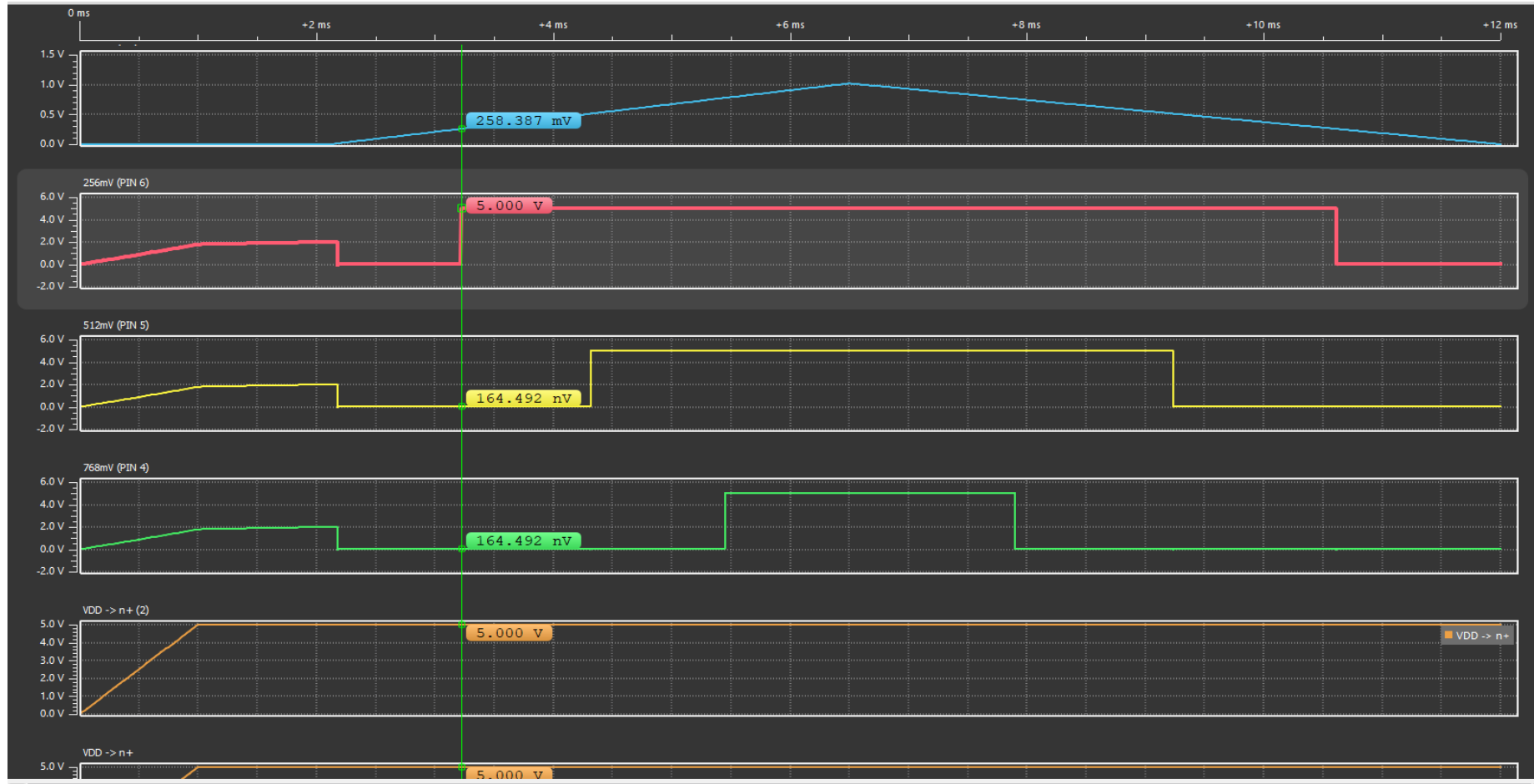
# SCHEMATIC AND MAPPING FOR TRAINING BOARD



SW4	1	LED1	Blue	PIN12
	2		Green	PIN10
	3		Red	PIN7
	4	LED2	Blue	PIN6
	5		Green	PIN5
	6		Red	PIN4
SW3	1	LED3	Blue	PIN19
	2		Green	PIN18
	3		Red	PIN17
	4	LED4	Blue	PIN16
	5		Green	PIN15
	6		Red	PIN13

# DESIGN DEMONSTRATION #1 WITH REAL HARDWARE

## Simulation Results with Markers

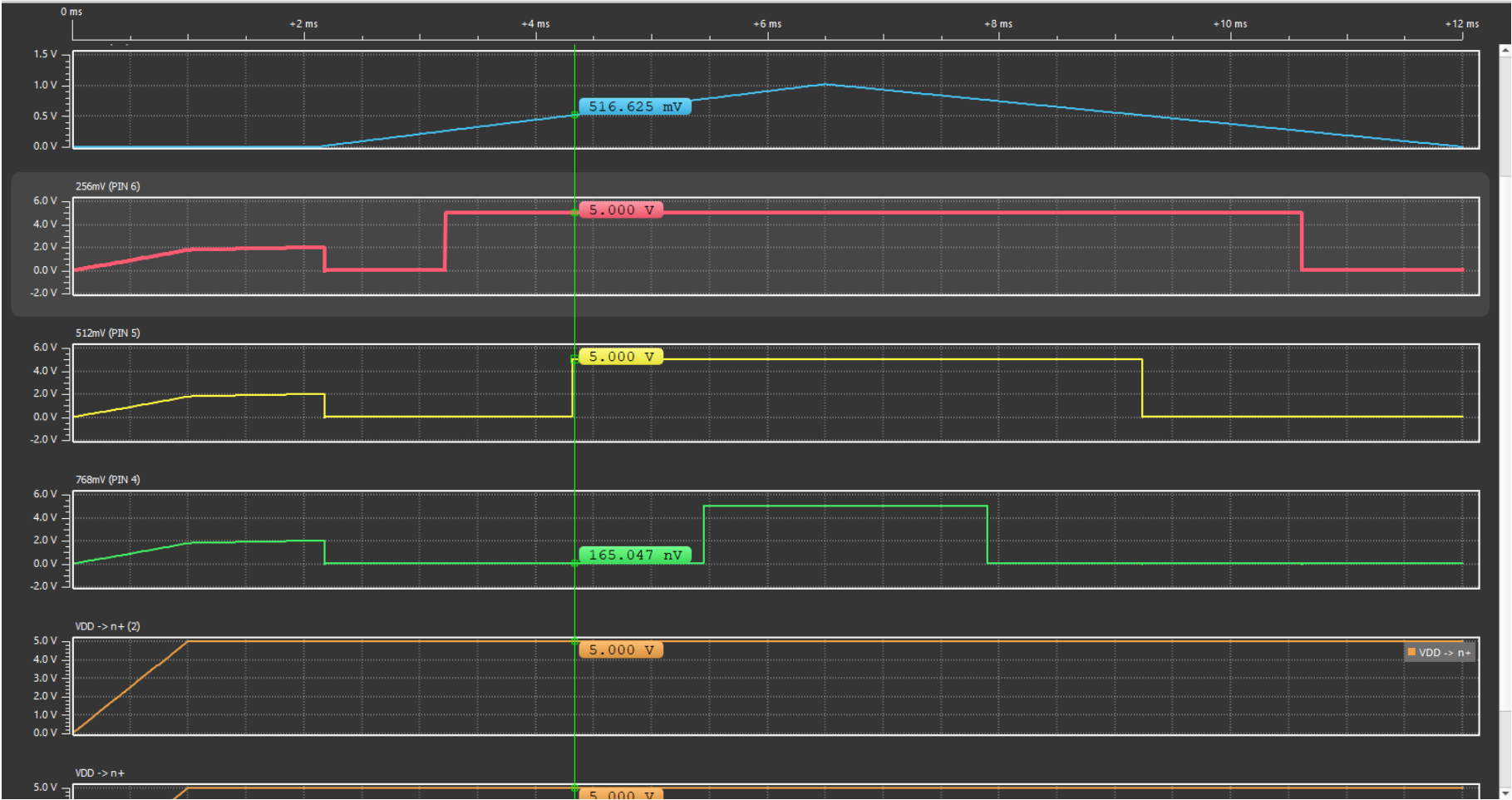


## Simulation results

- $V_{IN} > 256 \text{ mV}$
- $V(\text{PIN } 6) = 5 \text{ V}$
- $V(\text{PIN } 5) = 0 \text{ V}$
- $V(\text{PIN } 4) = 0 \text{ V}$
- Green LED ON @ Training Board
- TP6 LED is ON

# DESIGN DEMONSTRATION #1 WITH REAL HARDWARE

## Simulation Results with Markers



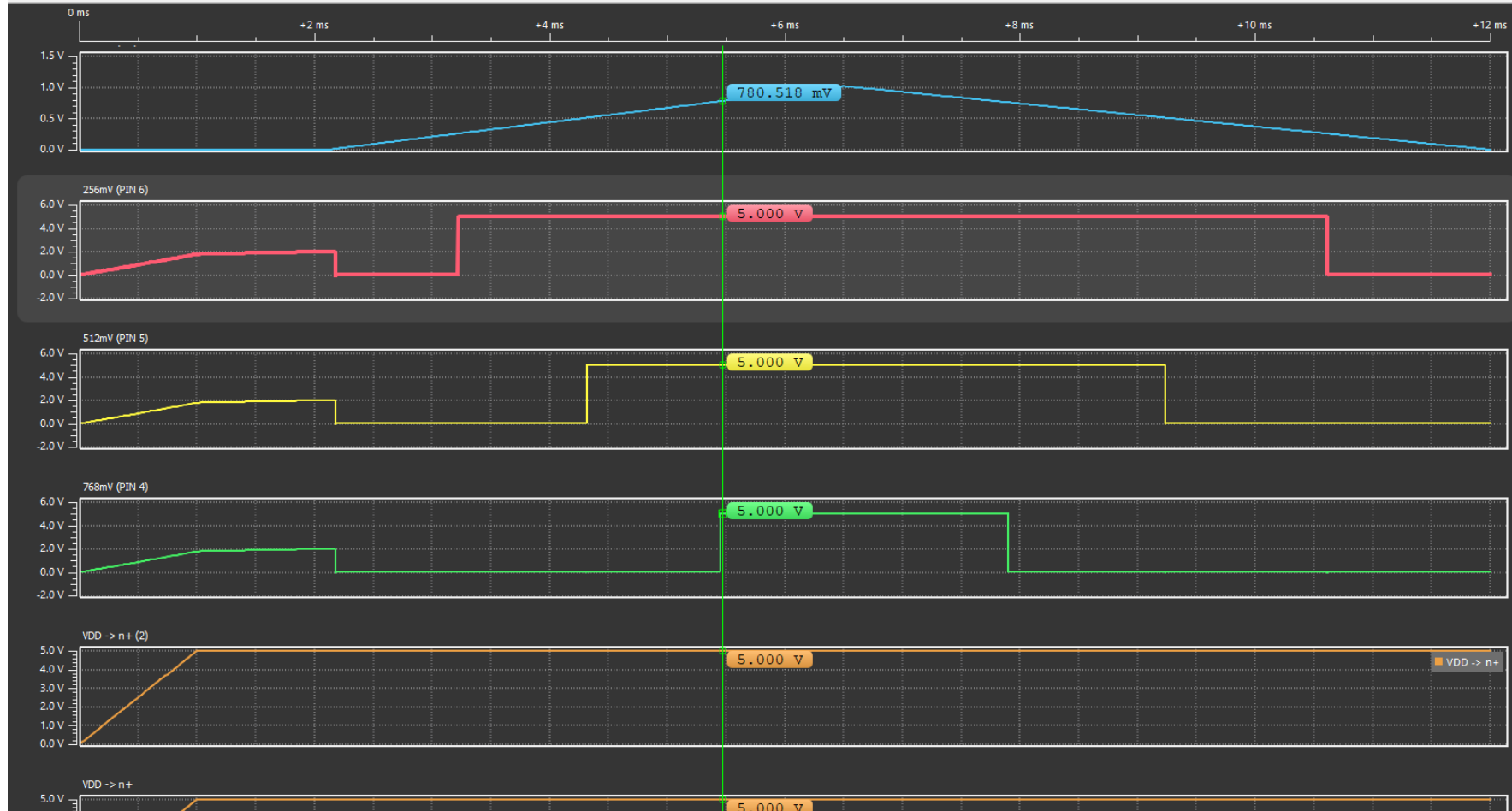
### Simulation results

- VIN > 512 mV
- V (PIN 6) = 5 V
- V (PIN 5) = 5 V
- V (PIN 4) = 0 V
- Red LED ON @ Training Board
- TP6 LED is ON
- TP5 LED is ON



# DESIGN DEMONSTRATION #1 WITH REAL HARDWARE

## Simulation Results with Markers

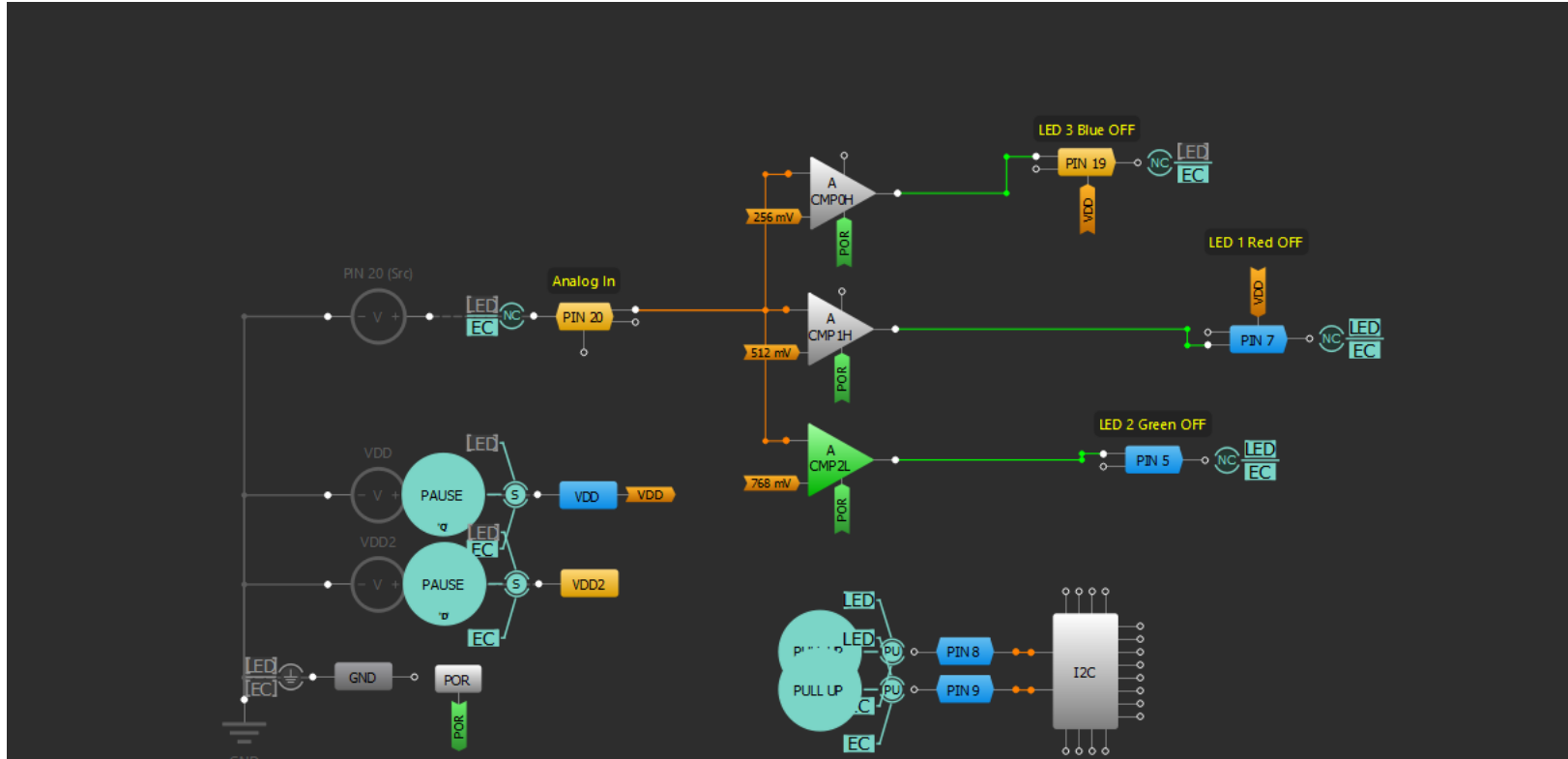


## Simulation results

- VIN > 768 mV
- V (PIN 6) = 5 V
- V (PIN 5) = 5 V
- V (PIN 4) = 5 V
- No LED ON @ Training Board
- TP6 LED is ON
- TP5 LED is ON
- TP4 LED is ON

# DESIGN DEMONSTRATION #2 WITH REAL HARDWARE

## Linking the PINs to other LEDs (Emulation Mode)

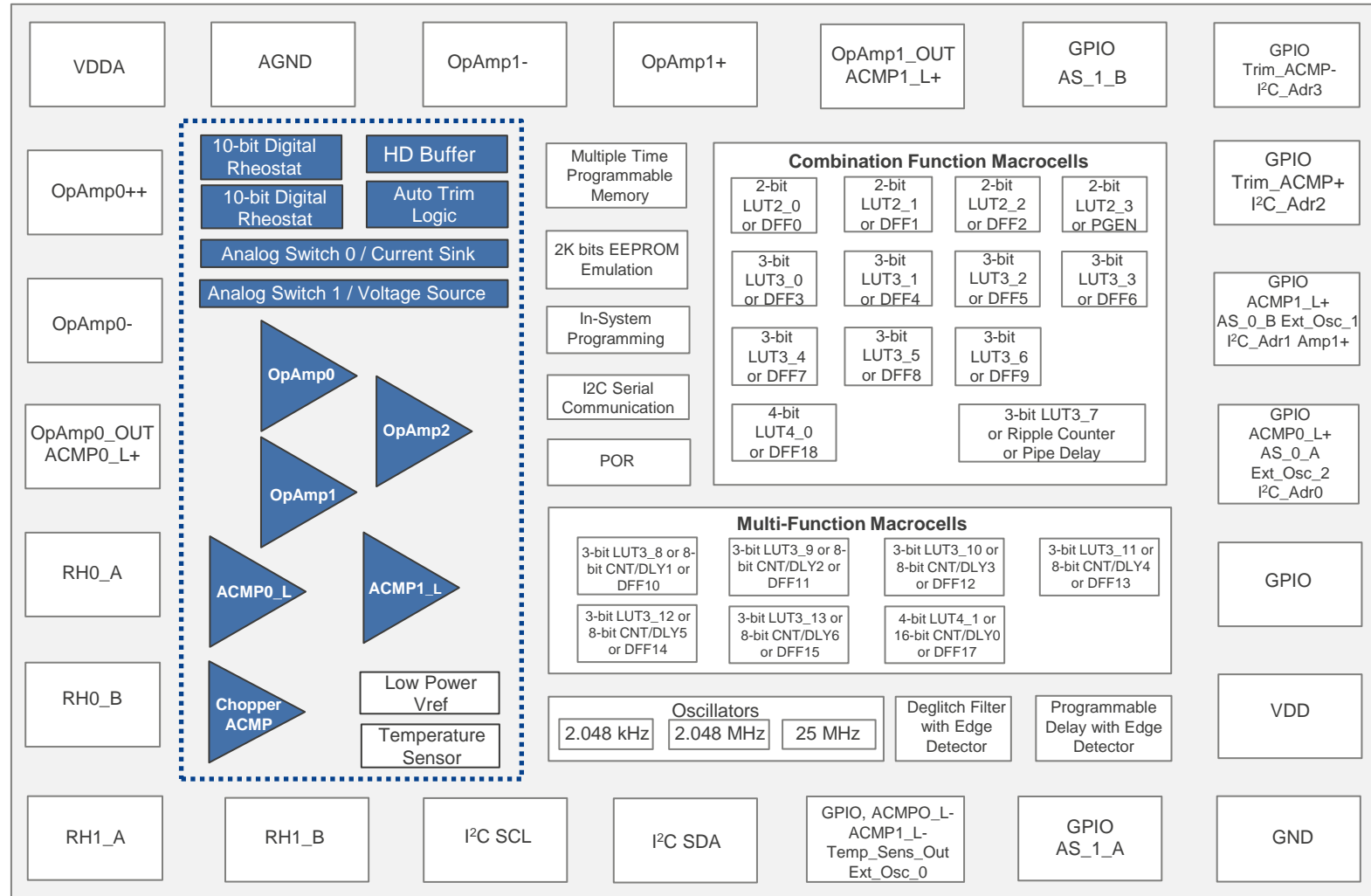


- PIN 19 = LED 3 Blue OFF
- PIN 7 = LED 2 Green OFF
- PIN 5 = LED 1 Red OFF
- TP7 LED is ON
- TP5 LED is ON

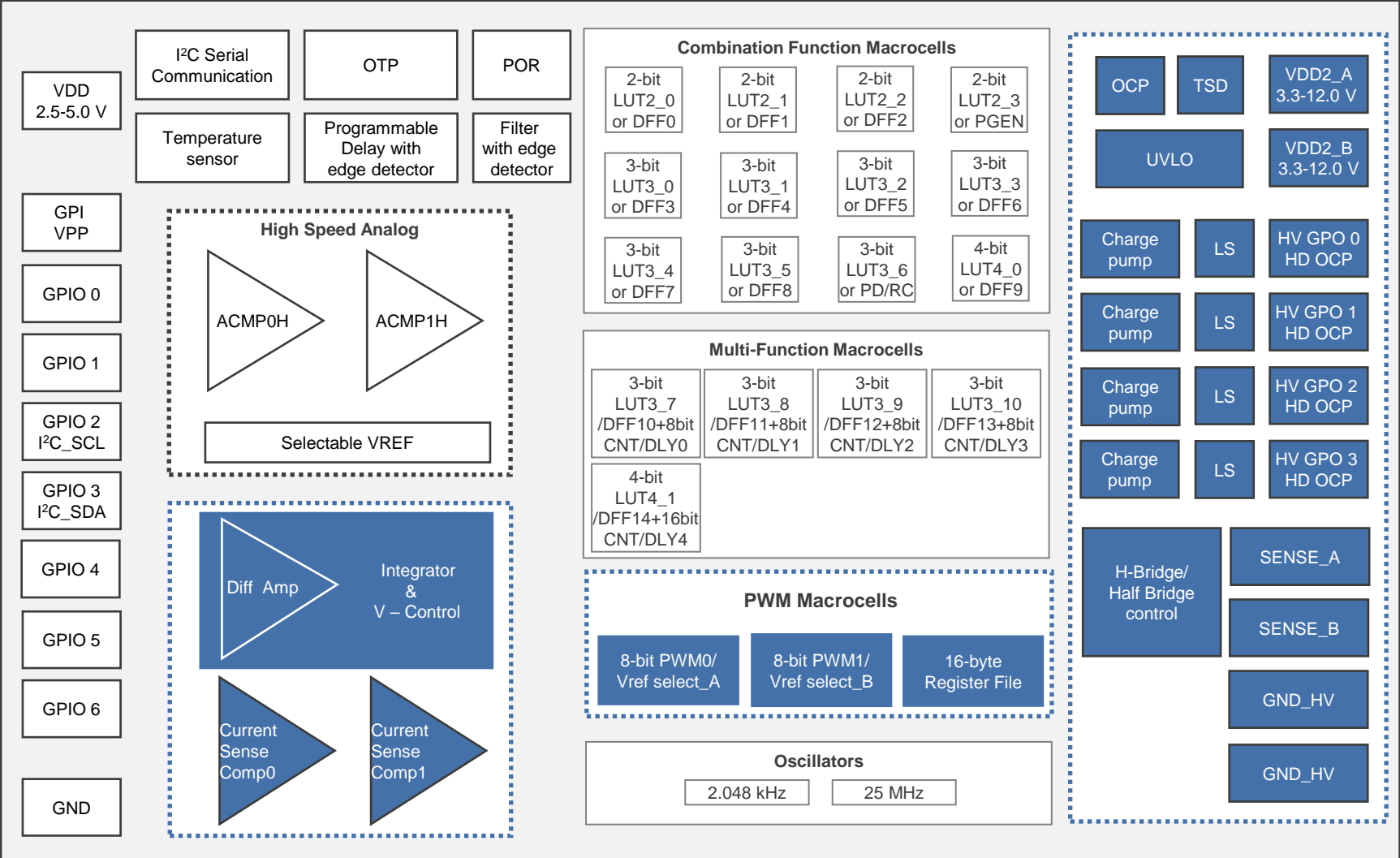
Input PIN 20 is variable (POTI)

# GREENPAK MACRO CELLS (EXAMPLES)

# EXAMPLE: ANALOGPAK: SLG47004: BLOCK DIAGRAM

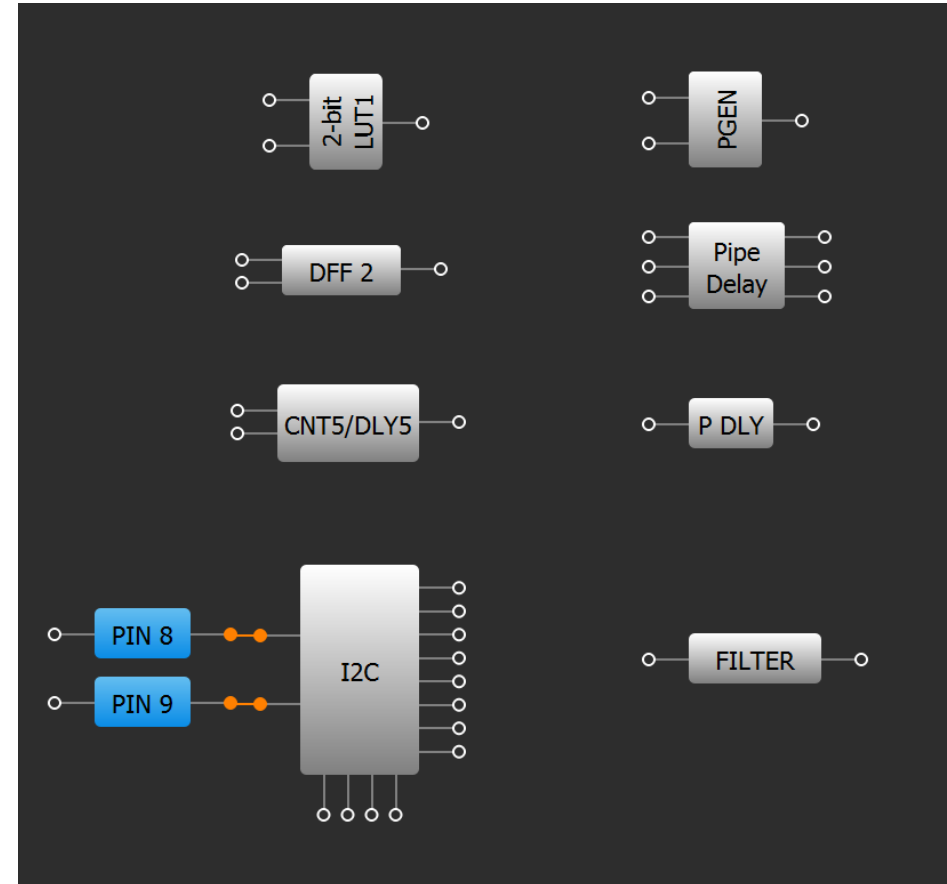


# EXAMPLE: HVPAK:SLG47105 BLOCK DIAGRAM



# DIGITAL MACROCELLS

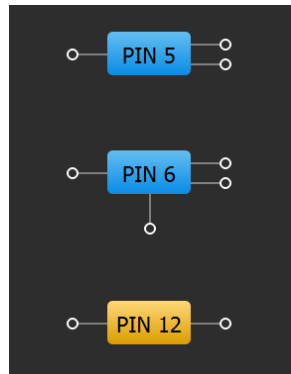
- Common Digital Macro cells
  - Look-Up Tables (LUTs)
  - D Flip-Flop (DFF) / Latch
  - Counter / Delay (CNT/DLY)
- Communication
  - I<sup>2</sup>C (many devices)
  - SPI (select devices)
- Less Common
  - Pattern Generator (PGEN)
  - Pipe Delay
  - Programmable delay (PDLY)
  - Filter / Edge Detector



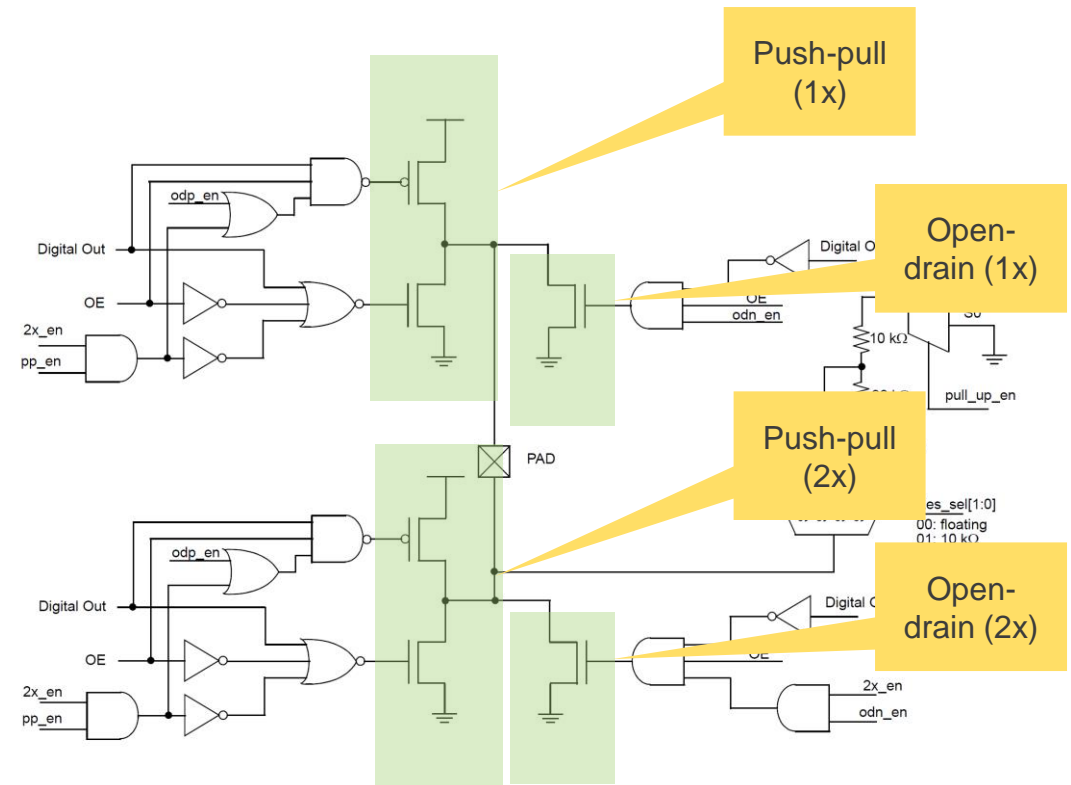
# I/Os

## Most I/Os in GreenPAK devices are very flexible

- Various output modes [Push-pull (1x or 2x), Open-drain (1x or 2x) or Analog-Output]
- Various input modes [Digital-In, Digital-In with Schmitt trigger, Low Voltage Digital-In and Analog-In]
- Some I/Os support Output Enable
- Some I/Os support level shifting

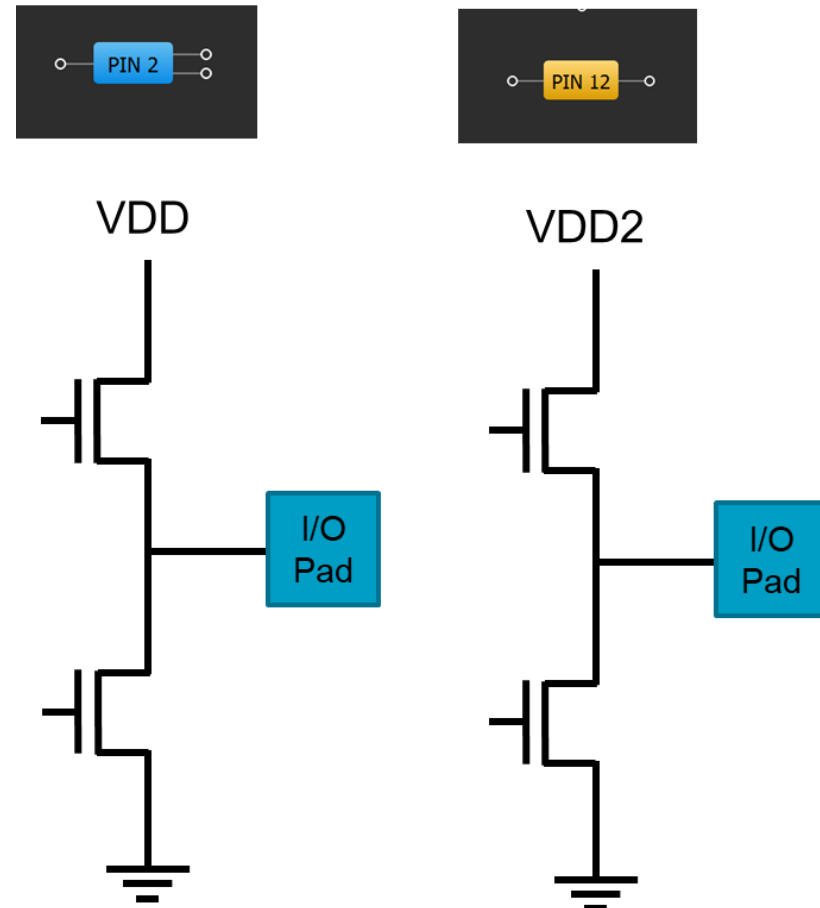


## Typical I/O Structure



# LEVEL SHIFTING

- GreenPAK devices with VDD2 have some I/O pins tied to VDD2
- You can see this by the color of the Pin icon
- This makes level shifting applications very easy to implement
- Some of the devices have VDD2

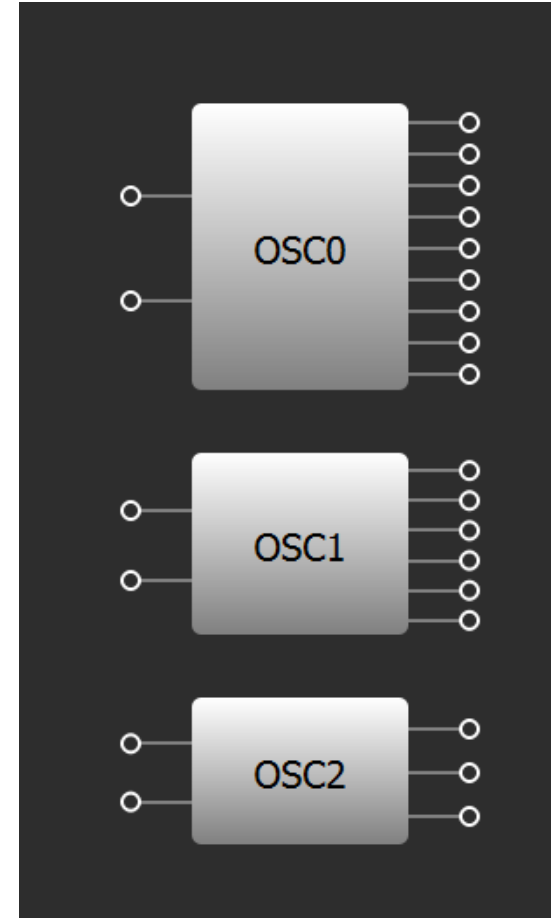




# OSCILLATORS

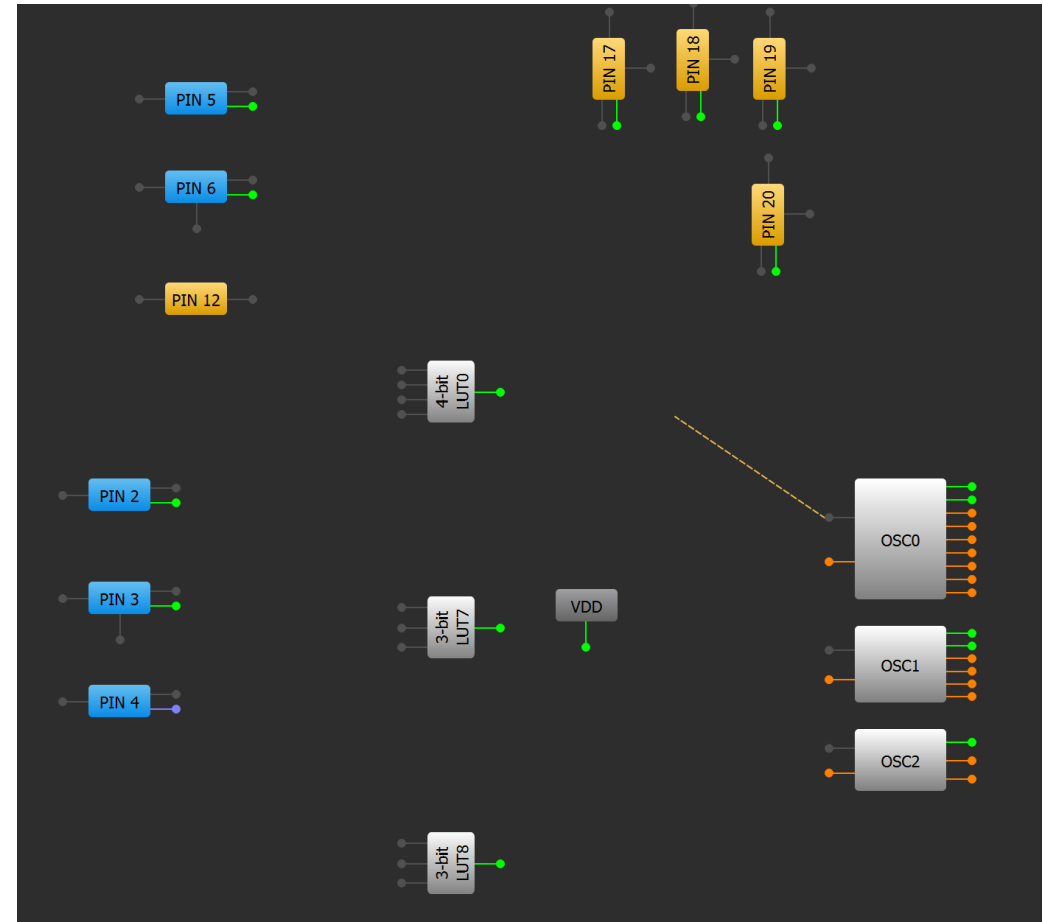
---

- Most GreenPAK devices have at least two oscillators
- Newest devices have three oscillators, i.e., SLG46824/826 have three oscillators
  - 2KHz low speed, low power oscillator
  - 2MHz medium speed
  - 25MHz high speed
- Auto-power on option allows you to turn off the oscillator when the clock is not needed
  - Great way to save power
- Oscillator outputs have several pre-dividers to allow you flexibility in clocking



# INTERCONNECTIONS

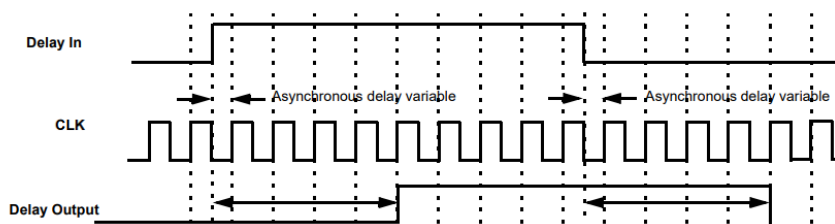
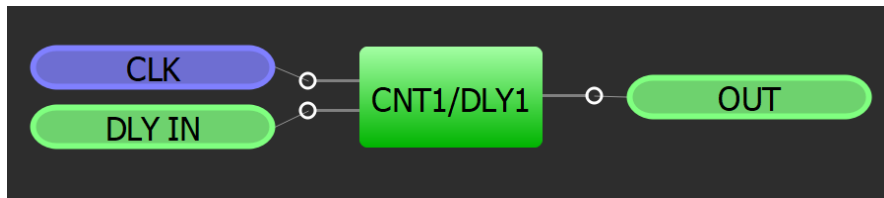
- Interconnection is easy
- System will guide you on which connections you can make
- When you click on any connection point, the system:
  - Highlights all available connections in green
  - Gives you a “rubber band” connection that you can stretch to any of these green connection
  - This results in a green wire to show you interconnections you have made



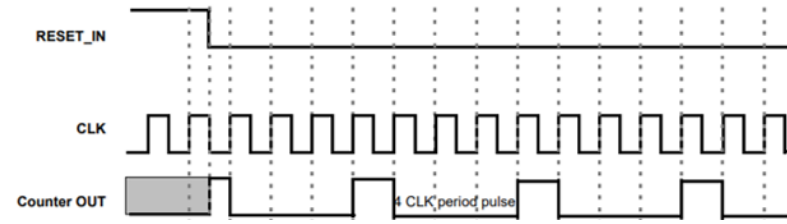
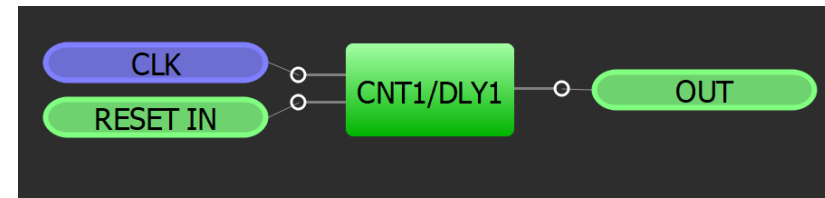
# COUNTER DELAY (CNT/DLY) BLOCKS

- CNT/DLY macrocells allow diverse customization of timing sequences
- Configuration modes to match unique behavior
  - Delays
  - One-shot
  - Frequency Detect
  - Reset Counter
  - Edge Detect
  - Delayed Edge Detect

## Delay Mode (Both Edges)

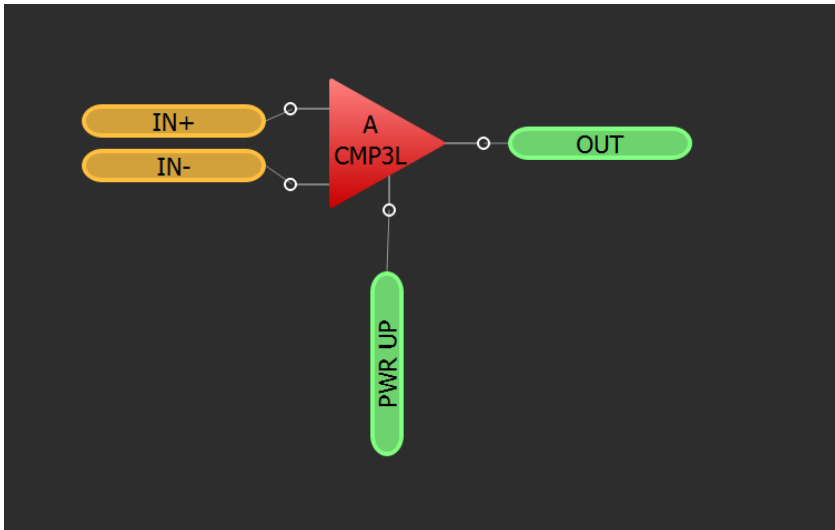


## Reset Counter Mode (High-level Reset)



# ACMPs

- ACMPs offer easy and integrated way to include analog input functions in your GreenPAK design
  - ACMPs in GreenPAK optimized high integration – including selectable internal voltage references
  - Power Up (PWR UP) signal input allows for powers savings by turning off the ACMPs



Properties

**A CMP3L**

100uA pullup on input: None

Hysteresis: Disable

IN+ gain: Disable

**Connections**

IN+ source: PIN 17 (IO11)

IN- source: 32 mV

**Information**

Typical ACMP thresholds

V_IH (mV)	V_IL (mV)
32	32

Power ctrl. settings

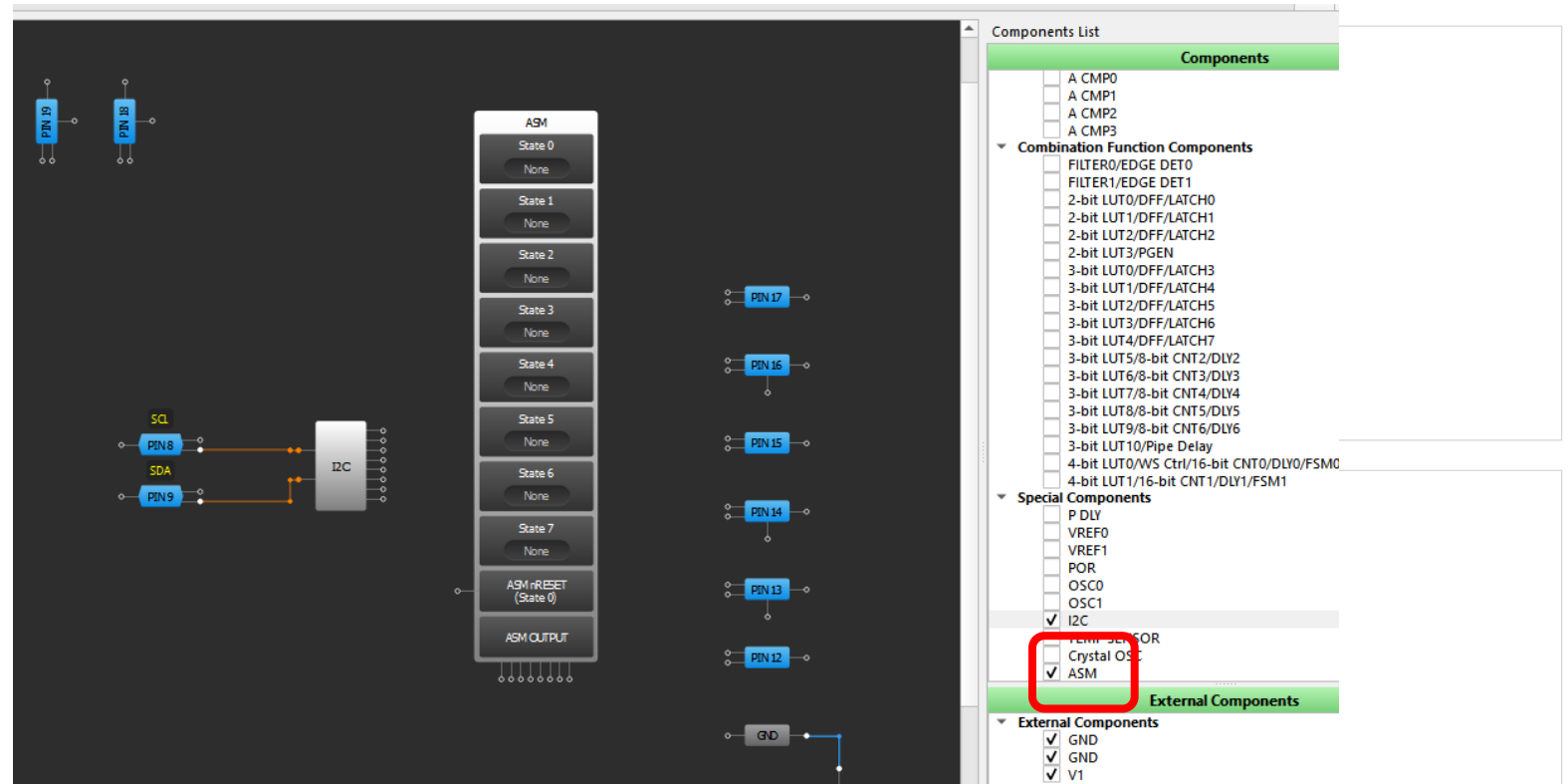
Apply

- 100 $\mu$ A pullup on input
- Hysteresis
- Gain
- In+ Source
- In- Source
- Internal voltage reference goes from 32mV to 2016mv
  - Step size is 32 mV
- External voltage reference is also an option

# ASYNCHRONOUS STATE MACHINE

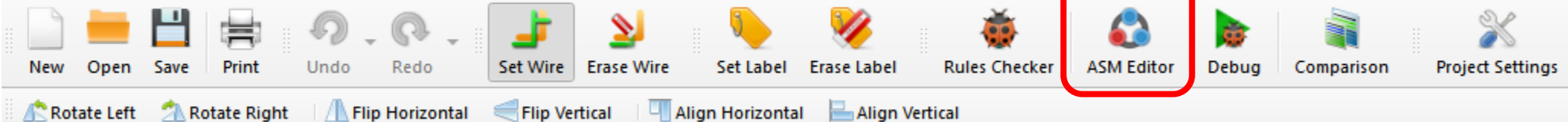
Some Greenpaks features an ASM (asynchronous state machine) block (e.g. SLG46537)

The ASM is convenient way to create power sequencer function.

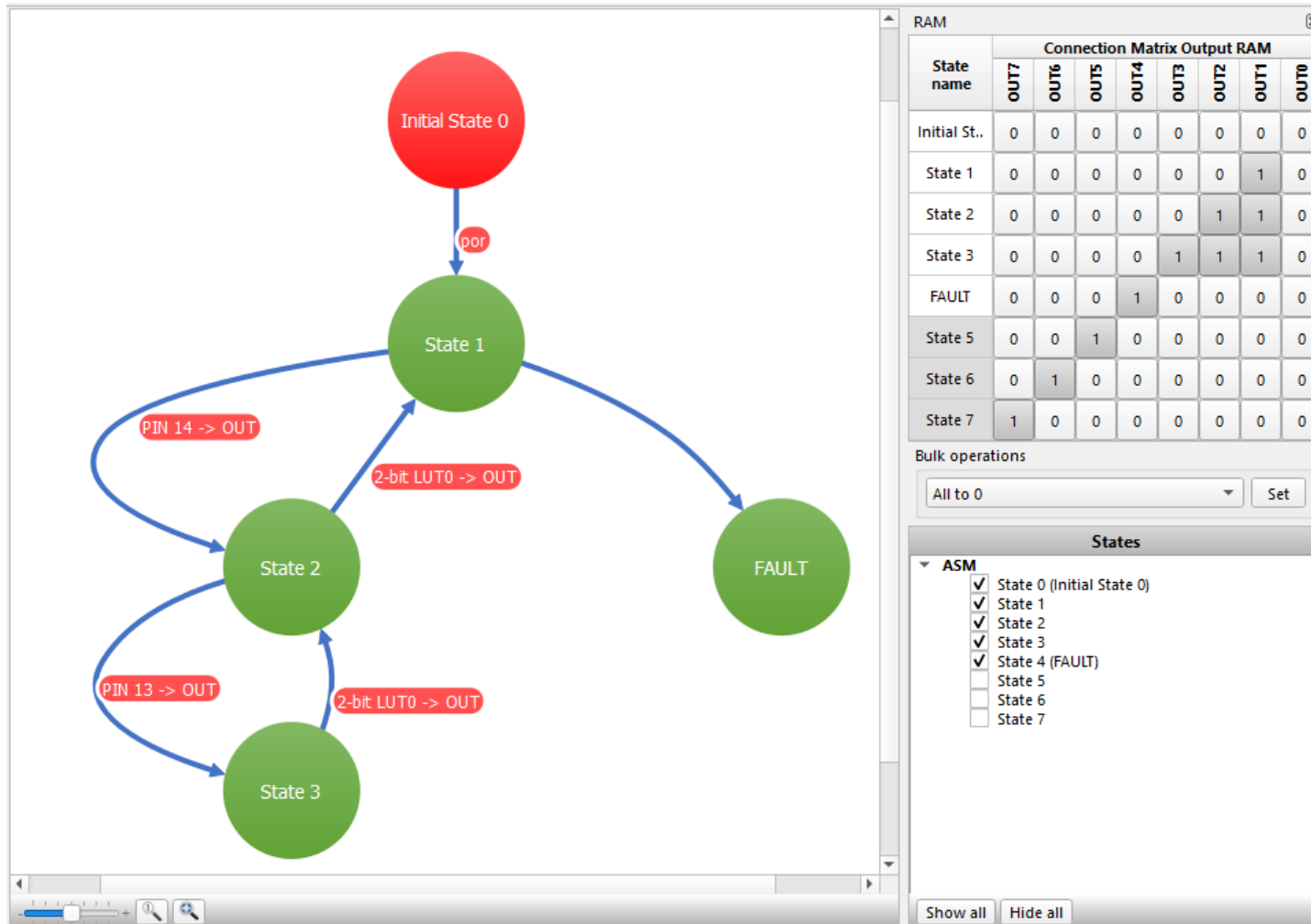


[SLG46537V] - GreenPAK Designer v.6.32

File Edit View Tools Options Help



# ASYNCHRONOUS STATE MACHINE: DESIGN VIEW



Define your states with Look up tables and in a flow chart

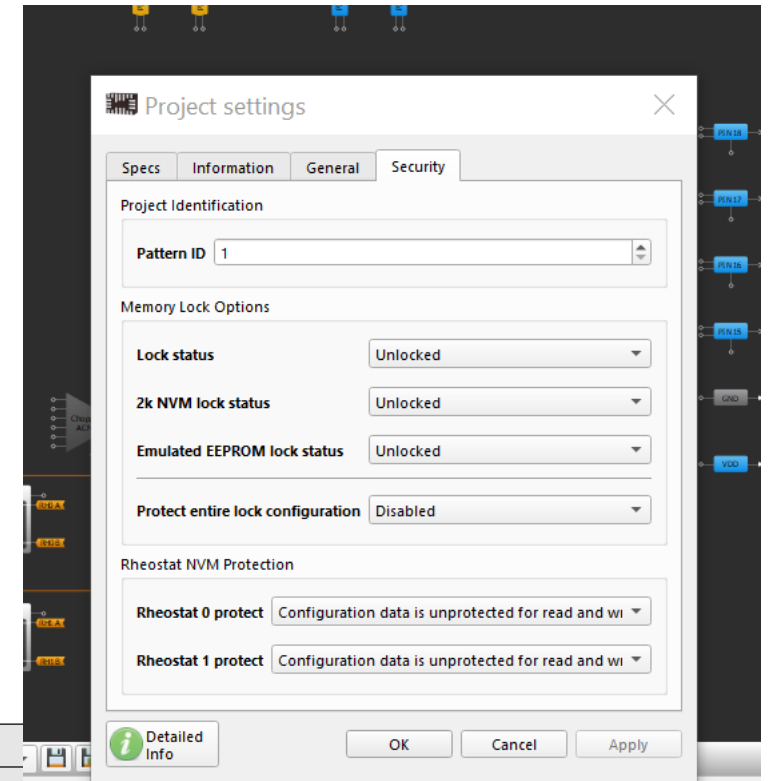
# DESIGN SECURITY

# DESIGN SECURITY

- Greenpaks allows a portion or the entire Register and NVM to be inhibited from being read or written/erased
- Customer specific designs can be “hidden” inside a Greenpak,
- looks like a “Black Box” from outside
- It’s up to the customer’s choice how much he would like to “hide” of his specific design
- Impedes “Reverse Engineering” of your design
- Can be easily done in “Project Settings” in the Go Configure Software Hub

Table 65: Read/Write Register **Protection** Options

Configurations	Protection Modes Configuration									Test Mode	Register Address
	Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/Write		
RPR[1:0]	00	01	00	01	01	10	10	00	10		
RPR[3:2]	00	00	01	01	10	01	00	10	10		

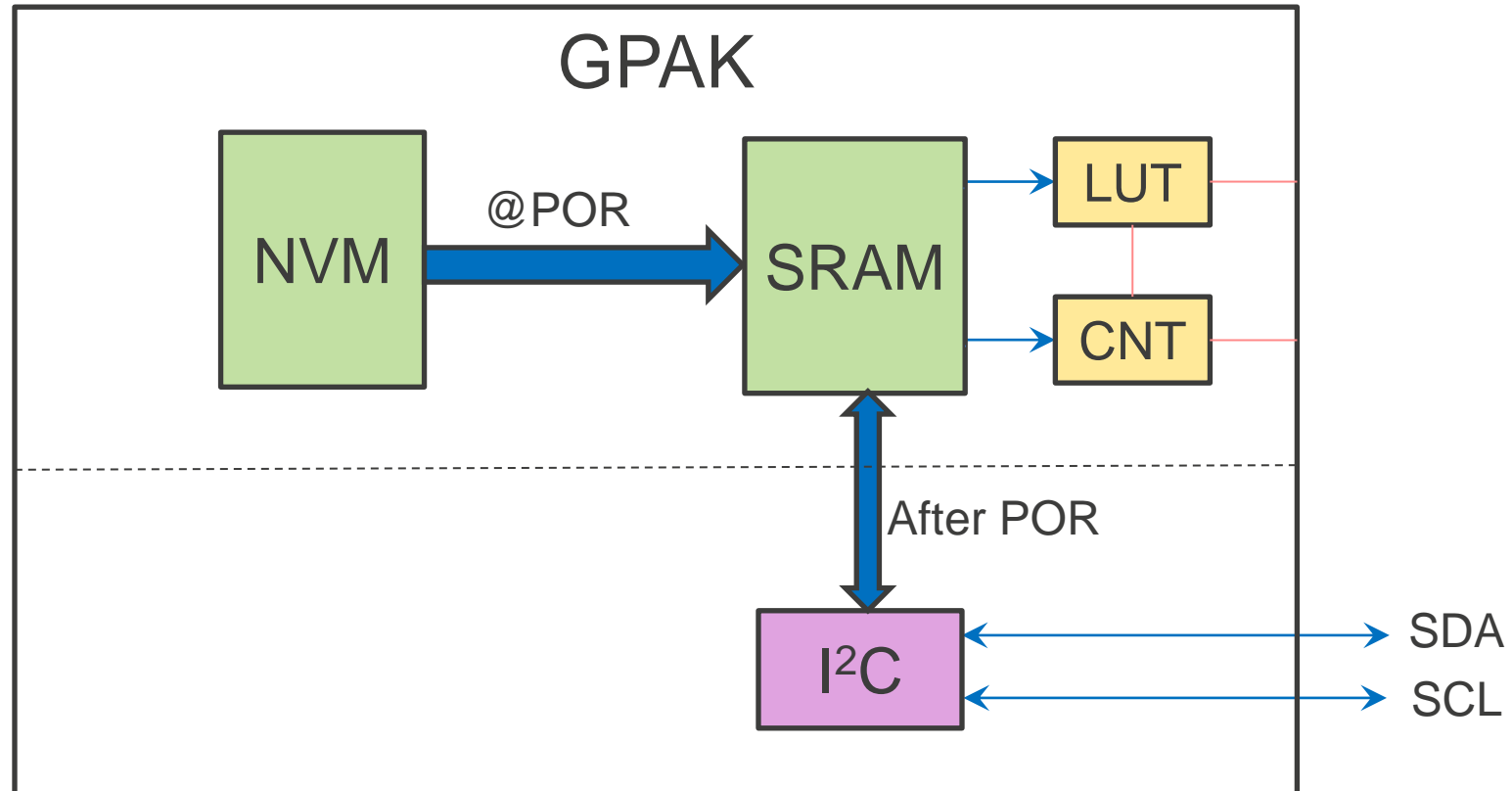
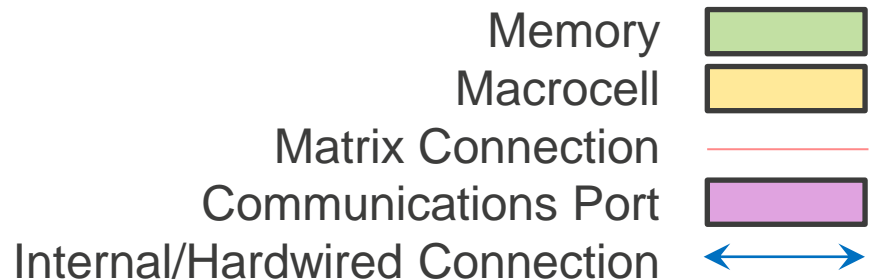





# GREENPAK – I2C BLOCK PRESENT

## Power Up Sequence

1. Apply VDD.
2. Internal POR goes active.
3. NVM copies to SRAM.
4. SRAM configures macrocells and matrix connections.
5. I2C can access SRAM to write changes. Changes are lost on POR or VDD cycle.



# DESIGN SECURITY: CUSTOM PART NUMBER: BASE PART VS CUSTOMER PART


Datasheet

**SLG47115**  
GreenPAK Programmable Mixed-Signal Matrix with High Voltage Features

The SLG47115 provides a small, low power component for commonly used Mixed-Signal and Full Bridge functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, the High Voltage Pins, and the macrocells of the SLG47115.

Configurable PWM macrocells in combination with Special High Voltage outputs will be useful for a motor drive or load drive applications. High Voltage pins allow to design smart level translators or to drive the high voltage high current load.

**Features**


- Two Power Supply Inputs:
  - 2.5 V (±8 %) to 5.0 V (±10 %) V<sub>DD</sub>
  - 5.0 V (±10 %) to 24.0 V (±10 %) V<sub>DD2</sub>
- Two High Voltage High Current Drive GPOs
  - Full Bridge Driver Option
  - Dual/Single Half Bridge Driver Option
- Slew Rate Modes:
  - Motor Driver Mode
  - Pre-Driver (MOSFET Driver) Mode
- High Drive GPOs with Sleep Function
- Low R<sub>DS(ON)</sub> High-side + Low-side resistance = 0.5 Ω typical
- 3 A Peak, 1.5 A RMS per Full Bridge<sup>[1]</sup>
- Current up to 3 A Peak, 1.5 A RMS per GPO/Half Bridge and up to 6 A Peak, 3 A RMS for two HV GPOs Connected in Parallel<sup>[1]</sup>
- Integrated Over Current/Short Circuit/Undervoltage-Lockout Protections
- SENSE Input that is connected to the Current Comparator for Current Control
- Fault Signal Indicator (OCP/UVLO/TSD/)
- Differential Amplifier with Integrator and Comparator for Motor Speed Control Function
- Current Sense Comparator with Dynamical Vref Mode
- Two High-Speed General Purpose ACMPs
  - Modes: UVLO, OCP, TSD, Voltage Monitor, Current Monitor
- One Voltage Reference (Vref) Output
- Five Multi-Function Macrocells


- Four Selectable DFF/LATCH/3-bit LUTs + 8-bit Delay/Counters
- One Selectable DFF/LATCH/4-bit LUT + 16-bit Delay/Counter
- Twelve Combination Function Macrocells
- Three Selectable DFF/LATCH or 2-bit LUTs
- One Selectable Programmable Pattern Generator or 2-bit LUT
- Six Selectable DFF/LATCH or 3-bit LUTs
- One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
- One Selectable DFF/LATCH or 4-bit LUT
- Two PWM Macrocells
- Flexible 8-bit/7-bit PWM Mode with the Duty Cycle Control
- 16 Preset Duty Cycle Registers Switching Mode for PWM Sine or Other Waveforms<sup>[2]</sup>
- Serial Communications
  - 1C Protocol Interface
- Programmable Delay with Edge Detector Output
- Additional Logic Function – One Deglitch Filter with Edge Detectors
- Two Oscillators (OSC)
  - 2.048 KHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor with ACMP Connected Output
- POR
- One Time Programmable Memory
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- 20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

**Applications**

- Smart Locks
- Personal Computers and Servers
- Consumer Electronics
- Motor Drivers
- Toys
- HV MOSFET Drivers
- Video Security Cameras
- LED Matrix Dimmers

[1] Power dissipation and thermal limits must be observed. See Section 3.3 Recommended Operating Conditions.  
[2] For all PWM features see Section 13. Pulse Width Modulation Macrocell.

R19DS0118EU0111 Rev.1.11  
Sep 23, 2022

Page 1  
© 2022 Renesas Electronics



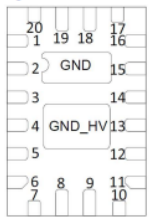
**SLG4BF45665**

  
**GreenPAK™**  
**Camera shutter Module**

**General Description**

The SLG4BF45665 provides a small, low power component for commonly used Mixed-Signal and H-Bridge functions. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices. Configurable PWM macrocells in combination with Special High Voltage outputs will be useful for a motor drive or load drive applications. High Voltage pins allow to design smart level translators or to drive the high voltage high current load.

**Pin Configuration**



**STQFN-20L  
(Top View)**


**Features**

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package
- Four High Voltage High Current Drive GPOs
- Current up to 1.5A RMS per GPO/ H-Bridge
- Differential Amplifier with Integrator
- Two Current Sense Comparators
- Two PWM Macrocells

**Output Summary**  
2 Outputs - High Drive Push Pull

**Pin name**

Pin #	Pin name	Pin #	Pin name
1	VDD	11	VDD2_B
2	NC	12	PGND
3	NC	13	GND
4	GND	14	NC
5	PGND	15	SCL
6	VDD2_A	16	SDA
7	OUT1	17	NC
8	OUT2	18	GND
9	NC	19	NC
10	NC	20	NC

SLG4BF45665\_DS\_r010  
SLG4BF45665\_GP\_r001

Rev 0.10  
Revised March 25, 2022

- **Base device IC datasheet on left**
  - Base datasheets have default device information
- **Customer specific part number & custom datasheet right**
  - Customer specific part number is unique to GreenPAK IC design
- **Customizable datasheet**
  - Tailored to customer request (i.e. remove or add specific data such as tables or figures)
- **Purchasable only by customer**
  - Only customer who owns design can purchase part
  - Need approval from customer to sell to non-customer entity (CM, 3<sup>rd</sup> parties, etc.)

# GREENPAK RESOURCES

# PRODUCT SELECTION TABLE

## Product Selection Table

Hide Filters

Reset Full Screen Export Tips

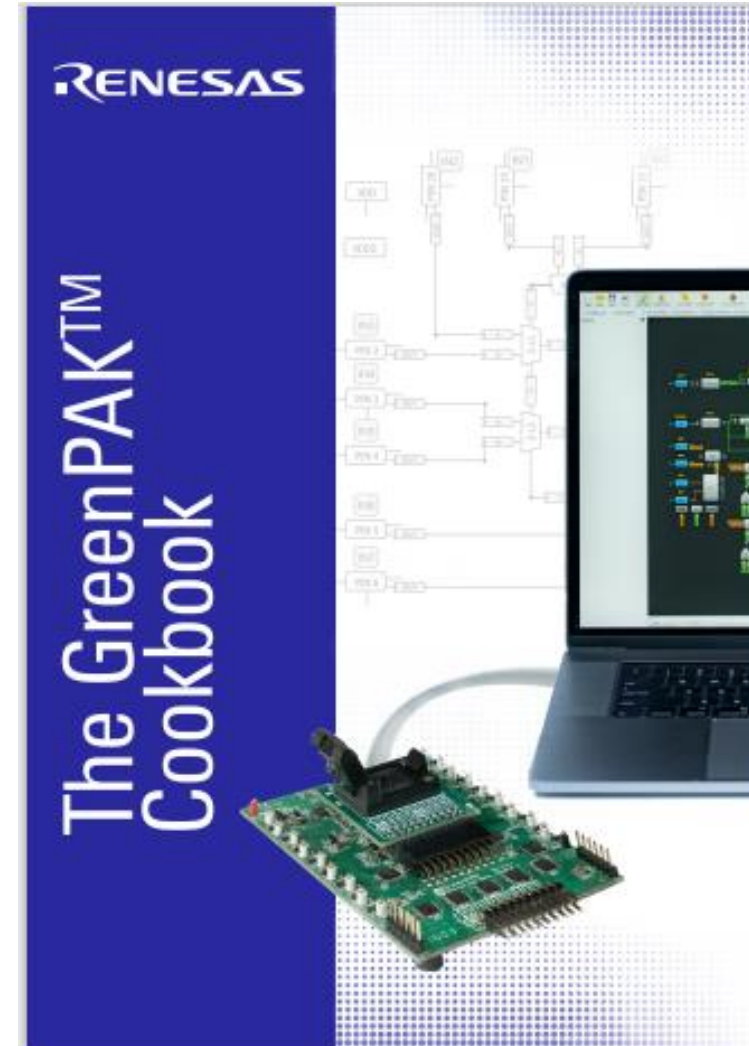
Part Number	Special Features	GPIOs (#)	Normal
<b>Part Count: 7</b> <input checked="" type="checkbox"/> (46) Featured Products <input type="checkbox"/> (0) Additional Products <input type="text" value="Automotive"/>	<input type="checkbox"/> 1x H-/2x Half- Bridge, 2x PWM, CCMP, Int&Diff Amp, Pattern Generator <input type="checkbox"/> 2x H-/4x Half- Bridge, 2x PWM, 2x CCMP, Int&Diff Amp, Pattern Generator <input type="checkbox"/> 2x Op Amp or 1x In-Amp, 2x Rheostat, 2x An Switch, 2-Ch Auto-Trim, EEPROM, Pattern Generator <input type="checkbox"/> 2x P-FET (44Ω, 2A) OR <input type="checkbox"/>	<input type="text" value="≤ 28"/> <input type="text" value="≥ 0"/>	<input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> <input type="checkbox"/> OR
<input type="checkbox"/> <a href="#">SLG46538-A</a> Automotive GreenPAK™ Programmable ...	ASM (8 states), Pattern Generator	17	
<input type="checkbox"/> <a href="#">SLG46620-A</a> Automotive GreenPAK Programmable M...	3x PWM, ADC (8-bit, SAR), 2x DAC, Pattern Generator	18	
<input type="checkbox"/> <a href="#">SLG46625-A</a> Automotive GreenPAK Programmable M...	3x PWM, ADC (8-bit, SAR), 2x DAC, Pattern Generator	18	
<input type="checkbox"/> <a href="#">SLG46827-A</a> Automotive GreenPAK™ Programmable ...	Pattern Generator	17	

[GreenPAK™ Programmable Mixed-signal Products | Renesas](#)

# GREENPAK COOKBOOK

---

- Our Cookbook has **OVER 90** applications & techniques references for design with GreenPAK
- The design files are downloadable
- [Greenpak Cookbook](#)
- Good Approach to start your design
- Search for the application and extent your design with the building blocks needed

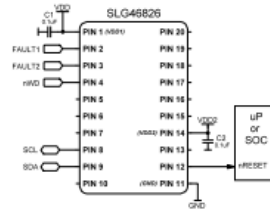


# GREENPAK COOKBOOK AND APPLICATION NOTES

The GreenPAK Cookbook RENESAS

### Application: System Reset

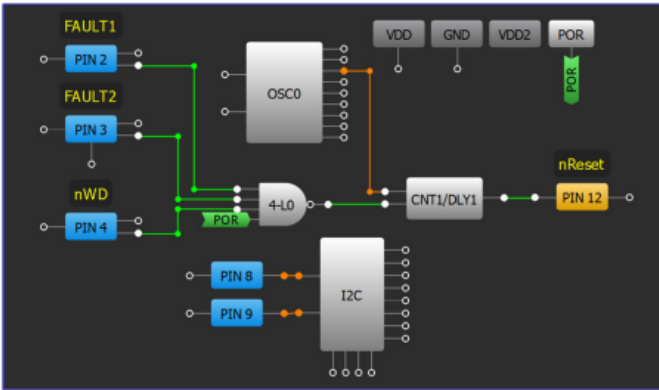
System Reset ICs are used to provide a reset to a microprocessor during faults, manual resets, brown-outs and more.



**Ingredients**

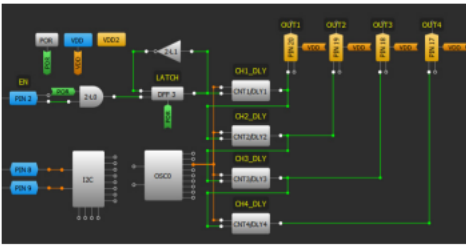
- Any GreenPAK
- No other components are needed

### GreenPAK Diagram

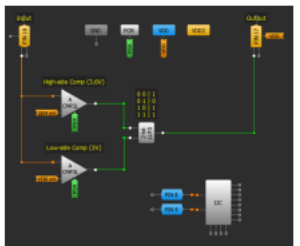


### Design Steps

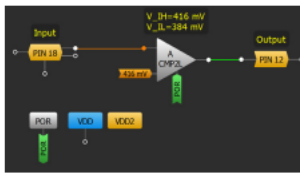
1. Configure an I/O as an input for each input signal.
2. Add LUT logic to create a HIGH signal when any of the lines are active. The logic is dependent on whether each signal is active-high or active-low.
3. Configure a CNT/DLY block to "One shot" mode, with Edge select configured to "Rising." Set the Counter data to create the desired length of pulse. For an active-low pulse change the Output polarity to "Inverted (nOUT)."
4. Connect the CNT/DLY block's output to an output pin.



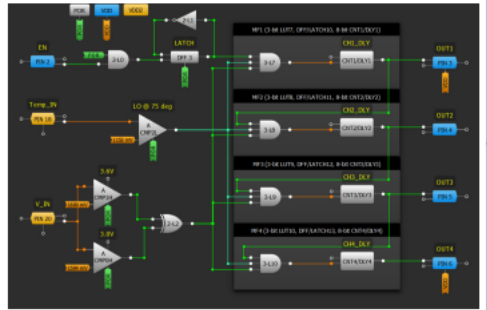
Power Sequencing



Window Comparator



Overtemperature Detection



Unique Solution

Both can be used together to create

- New features
- New applications

# EXAMPLES FOR APPLICATION NOTES

## Adjustable Filter



### Low Pass Filter Solution:

- Sallen-Key Topology
- Cutoff Frequency
  - $F_{C1} = 100 \text{ kHz}$
  - $F_{C2} = 1 \text{ MHz}$
- Manual Trim Controlled by GreenPAK Digital Logic

Application Note

## Tracking ADC



### I<sup>2</sup>C Controlled ADC:

- Potentiometer Mode Configuration
- $V_{IN}$  Tracking using the Auto-Trim Feature
- I<sup>2</sup>C-Accessible Digital Value

Application Note

## Sigma-Delta ADC



### Precision ADC:

- 16-bit resolution
- 0.5 mV offset, 0.009% gain error, 2LSB (max) INL
- 1.95 sps
- I<sup>2</sup>C-Accessible Digital Value

Application Note

## Pressure Sensor



### Wheatstone Bridge AFE:

- Auto-Trim Algorithm for Gain Tuning and Offset Compensation
- $V_{AN}$  & 2.048V Reference Solutions
- Error Analysis

Application Note

## Heart Rate Monitor



### Transimpedance (TIA) Amplifier for Photodiode Sensing:

- LED Driving
- Sample & Hold Circuit
- AC Coupling with DC Bias Ambient Light Compensation
- Non-Inverting Amplification

Application Note

# HVPAK APPLICATION NOTES

---

## Smart Home

- [AN-CM-296 Smart Lock Motor Driver with Voltage Regulation](#)
- [AN-CM-298 Smart Lock Motor Driver with Battery Discharge Compensation](#)
- [AN-CM-301 LED Lamp Driver](#)
- [AN-CM-316 Automatic Air Freshener](#)
- [AN-CM-332 Smart PWM Fan Driver](#)
- [AN-CM-339 Ultrasonic Humidifier](#)
- [AN-CM-340 Brightness-Controlled Lamp with Motion Sensor](#)
- [AN-CM-344 Remote TX and RX Control System for Toys](#)
- [AN-CM-345 Ultrasonic Dog Chaser with Repelling Strobe Light](#)
- [AN-CM-353 Induction Heater with Variable Power Output](#)
- [AN-CM-359 Portable Washing Machine](#)

## Power

- [AN-CM-321 Class D Power Amplifier Using HV PAK](#)
- [AN-CM-322 Universal Class D \(UcD\) Power Amplifier](#)
- [AN-CM-337 Monolithic Battery Charger](#)

## Industrial/Consumer

- [AN-CM-295 Stepper Motor Driver](#)
- [AN-CM-315 High Voltage Zero-Crossing Relay Driver](#)
- [AN-CM-323 Simultaneous Dual Motor Control](#)
- [AN-CM-330 Ultrasonic Qualitative Distance Estimation Sensor](#)
- [AN-CM-342 Power Saving Solenoid Driver](#)



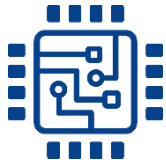
# DESIGN RESOURCES - USEFUL LINKS

---



## [Go Configure™ Software](#)

Schematic capture-like tool allowing design, configuration, and programming



## [GreenPAK Cookbook](#)

Outlines different techniques and provides completed applications for reference



## [Application Notes](#)

Resource of hundreds of design ideas

Collection of application specific collateral documenting design process for various solutions using GreenPAK



## [GreenPAK Forum](#)

is part of the Renesas Engineering Community

Online community for questions and support on GreenPAK



## [GreenPAK Partners](#)

Certified experienced GreenPAK third-party design partners



## [FAQs](#)

Knowledge base addressing common questions

# DESIGN RESOURCES - USEFUL LINKS

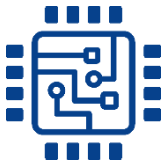
---



## [Renesas Academy](#)

You will find there GreenPAK Courses and Go Configure™ Software Hub Courses

## Non – Renesas Web sites



## [Hackster.io Greenpak Projects](#)

On Hackster IO Webside you will find 76 Greenpak projects



## [Hackaday IO](#)

On Hackaday IO Webside you will find 79 Greenpak projects



## [Greenpak Blog](#)

# DESIGNING WITH GREENPAK

# HOW TO GET STARTED

---

## Create a design on your own



Download our free Go Configure Software Hub

[Link](#)



Download our GreenPAK Cookbook

[Link](#)



Watch our training videos to get familiar with GreenPAK design

[Link](#)



Search our database for hundreds of example design files and app notes

[Link](#)



Program parts in minutes using the GreenPAK development board



Send us your design files for higher volume sampling

## Let us do the work, if you got stuck



Send your Disti FAE /Renesas FAE your IC requirements or system schematics and we will design a custom IC to suit your needs.

# WRAP-UP

# WHY IS GREENPAK POPULAR?



Design in minutes  
Prototype in hours



No NRE



No Production  
Commitment



14 Week  
Production  
Lead-time



Custom  
Datasheet



# WHERE CAN GREENPAK BE USED?

---

Many functions in many applications in many markets! Its universal...

## Functions

- Finite State Machine
- Timing Delays
- Counters
- Pulse Width Modulator
- Comparators
- Voltage Monitor
- Voltage Reference
- ADC
- Glue Logic
- Level Translation

## Applications

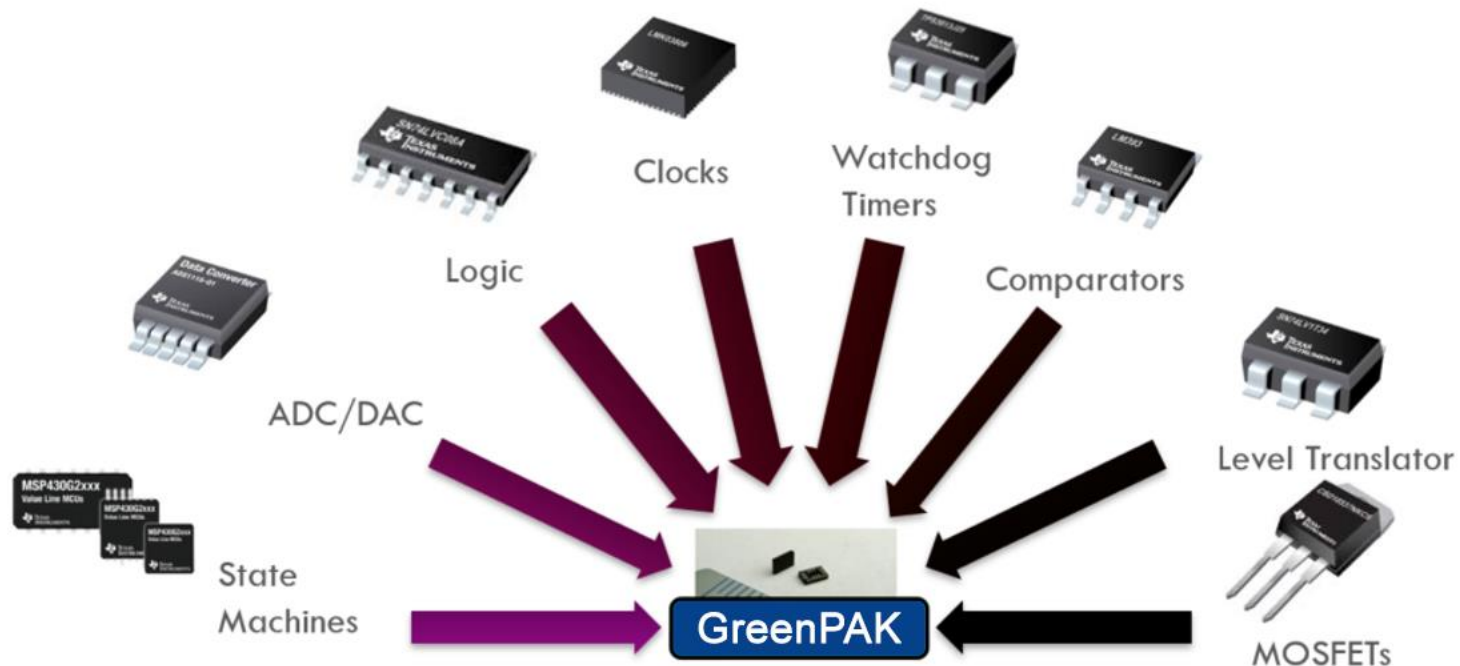
- Supervisory Circuits
- System Reset
- LED Control
- Motor & Fan Control
- Power Sequencing
- Voltage Detection
- Frequency Detection
- Sensor Interface
- Port Detection
- Temperature Control
- Coulomb Counter

## Markets

- Handheld Devices
- IoT / Wearable Electronics
- Computing & Storage
- Consumer Electronics
- Smart Home
- Networking & Communications
- Medical
- Industrial

# WHAT DOES GREENPAK REPLACE?

GreenPAK can replace simple discrete logic , analog comparators, low end 8-bit ADC's, etc. It can be used to implement non-standard variations of reset IC's and other ASSP's without tooling or NRE. This can support new variations of applications for customers who run into design issues.





# WHAT ARE THE GREENPAK BENEFITS?

---



## **Integrate and Differentiate**

Implement new features and functionality in one device as small as 1.0 mm x 1.2 mm



## **Shrink PCB Footprint**

Fewer components and less routing complexity



## **Reduce Power Consumption**

Extend battery life by powering fewer discrete devices and dynamically managing power within the GreenPAK



## **Adapt Design as Needed**

Adapt to changing requirements quickly and spin new prototypes in minutes



## **Faster Time to Market**

Development tools exploit the power of silicon without NRE charges and long lead times

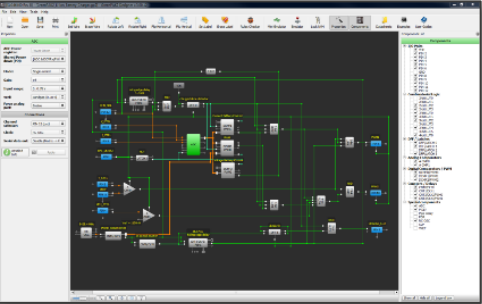


## **Secure**

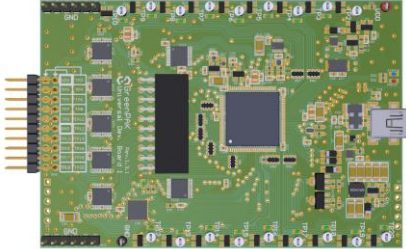
Circuit implementation is not visible to competition

# GREENPAK SOLUTION PLATFORM

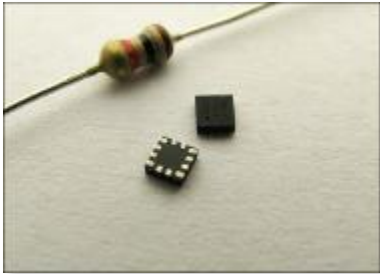
Design in MINUTES



Prototype in HOURS



Production in DAYS



The Choice is Yours



**Customers create solutions & program samples**

- Renesas provides un-programmed GreenPAK ICs
- Customer retains design control

**Renesas creates designs and provides samples**

- Customers communicate design requirements
- Design feedback and datasheet within 72 hours (typical)
- Custom part numbers assigned
- Delivery of programmed samples and tested production units

---

[Renesas.com](https://www.renesas.com)

# BACK UP SLIDES

# PRODUCTION GREENPAK FEATURE SETS

	SLG46108	SLG46127	SLG46116/7	SLG46110	SLG46120	SLG46140	SLG46169	SLG46170
# of GPIOs	6	6	7	8	10	12	12	12
Operating Voltage (V)	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0
Dual Supply (VDD2 1.8 V to VDD)	-	-	-	-	SLG46121 <sup>†</sup>	-	-	-
8-bit SAR ADC	-	-	-	-	-	1	-	-
Analog/Digital Comparators	-	2/0	2/0	2/0	2/0	2/3	2/0	-
Look Up Tables (LUTs)	4	4 Total	4 Total	4 Total	5 Total	8 Total	9 Total	15 Total
2-bit LUT	2	2	2	2	1	4	2	5
3-bit LUT	2	2	2	2	4	4	7	9
4-bit LUT	-	-	-	-	-	-	-	1
Combination Function Macro-cells	6 Total	6 Total	6 Total	6 Total	11 Total	8 Total	9 Total	2 Total
Selectable LUT/DFF/Latch	4	4	4	4	8	4	6	1
Selectable LUT/Pipe Delay	1	1	1	1	1	1	1	1
Selectable LUT/CNT/DLY	1	1	1	1	2	2	2	-
Selectable LUT/Pattern Gen	-	-	-	-	-	1	-	-
PWMs	-	-	-	-	-	3	-	-
Counters/Delays	3	3	3	3	2	2	5	8
DFF / Latch	-	-	-	-	-	2	-	6
Pipe Delay	-	8-stage	8-stage	8-stage	8-stage	16-stage	16-stage	16-stage
Programmable Delay	1	1	1	1	1	1	1	1
Internal Oscillator (Hz)	25k/2M	25k/2M	25k/2M	25k/2M	25k/2M	1.7k/25k/ 2M/27M	25k/2M	25k/2M
Load Switch	-	2 x 2 A P-FET	1.25 A P-FET	-	-	-	-	-
Asynchronous State Machine	-	-	-	-	-	-	-	-
Communication Interface	-	-	-	-	-	SPI	-	-
TQFN Part Number	SLG46108V	-	SLG46116V SLG46117V	SLG46110V	SLG46120V SLG46121V	SLG46140V	SLG46169V	SLG46170V
TQFN Package Size (mm)	1.0 x 1.2	-	1.6 x 2.5	1.6 x 1.6	1.6 x 1.6	1.6 x 2.0	2.0 x 2.2	2.0 x 2.2
MSTQFN Part Number	-	SLG46125M SLG46127M	-	-	-	-	-	-
MSTQFN Package Size (mm)	-	1.6 x 2.0	-	-	-	-	-	-

# PRODUCTION GREENPAK FEATURE SETS

	SLG46534	SLG46536	SLG46517	SLG46533	SLG46537	SLG46620	SLG46721	SLG46722
# of GPIOs	12	12	16	18	18	18	18	18
Operating Voltage (V)	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0	1.8 to 5.0
Dual Supply (VDD2 1.8 V to VDD)	SLG46535 <sup>†</sup>	-	-	-	SLG46538 <sup>†</sup>	SLG46621 <sup>†</sup>	-	-
8-bit SAR ADC	-	-	-	-	-	1	-	-
Analog/Digital Comparators	3/0	3/0	4/0	4/0	4/0	6/3	4/0	-
Look Up Tables (LUTs)	-	-	-	-	-	25 Total	9 Total	15 Total
2-bit LUT	-	-	-	-	-	8	2	5
3-bit LUT	-	-	-	-	-	16	7	9
4-bit LUT	-	1	-	1	-	1	-	1
Combination Function Macro-cells	17 Total	24 Total	17 Total	24 Total	17 Total	1 Total	9 Total	2 Total
Selectable LUT/DFF/Latch	8	15	8	15	8	-	6	1
Selectable LUT/Pipe Delay	1	1	1	1	1	-	1	1
Selectable LUT/CNT/DLY	7	7	7	7	7	-	2	-
Selectable LUT/Pattern Gen	1	1	1	1	1	1	-	-
PWMs	-	-	-	-	-	3	-	-
Counters/Delays	-	-	-	-	-	10	5	8
DFF / Latch	-	-	-	-	-	12	-	6
Pipe Delay	16-stage	16-stage	16-stage	16-stage	16-stage	2 x 16-stage	16-stage	16-stage
Programmable Delay	1	1	1	1	1	2	1	1
Internal Oscillator (Hz)	25k/2M/25M	25k/2M/25M	25k/2M/25M	25k/2M/25M	25k/2M/25M	1.7k/25k/ 2M/27M	25k/2M	25k/2M
Load Switch	-	-	2 x 2 A P-FET	-	-	-	-	-
Asynchronous State Machine	8-state	-	8-state	-	8-state	-	-	-
Communication Interface	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C	SPI	-	-
TQFN Part Number	SLG46534V SLG46535V	SLG46536V	-	SLG46533V	SLG46537V SLG46538V	SLG46620V SLG46621V	SLG46721V	SLG46722V
TQFN Package Size (mm)	2.0 x 2.2	2.0 x 2.2	-	2.0 x 3.0	2.0 x 3.0	2.0 x 3.0	2.0 x 3.0	2.0 x 3.0
MSTQFN Part Number	-	-	SLG46515M SLG46517M	SLG46533M	SLG46537M SLG46538M	-	-	-
MSTQFN Package Size (mm)	-	-	2.0 x 3.0	2.0 x 2.2	2.0 x 2.2	-	-	-

# PARAMETRIC TABLE EXAMPLE

## In-System Programmable

	SLG47105	SLG47115	SLG46824/SLG46826	SLG47004V	SLG47512/SLG47513
# of Pins / # of GPIOs	20/8 + 4 x HD	20/8 + 2 x HD	20/17	24/8	SLG47512 – 12/10 SLG47513 – 16/14
Operating Voltage, VDD (V)	2.3 to 5.5	2.3 to 5.5	2.3 to 5.5	2.3 to 5.5	1.0 to 1.65
Dual Supply, VDD2 (V)	3.0 to 13.2	4.5 to 26.4	1.71 to VDD	-	-
Dual Supply Version	-	-	-	-	-
Analog/Digital Comparators	4/0	3/0	4(2)/0	3(2)/0	2/0
Voltage Reference	Trimmed	Trimmed	Trimmed	Trimmed	Trimmed
Combo Function Macro-cells	12 Total	12 Total	11 Total	13 Total	15 Total
Multi-Function Macro-cells	5 Total	5 Total	8 Total	7 Total	8 Total
PWMs	2	2	-	-	-
Special Features	-	-	SLG46826: 2-kbit I <sup>2</sup> C compatible serial EEPROM emulation	2 Op Amps, 2 Rheostats, 2 analog switches, EEPROM	-
Counters/Delays	5	5	-	-	-
DFF / Latch	15	15	-	-	-
3-Output Pipe Delay	16-stage	16-stage	16-stage	16-stage/0	-/14
Programmable Delay	Yes	Yes	Yes	Yes	Yes
Internal Oscillator (Hz)	2k/25M	2k/25M	q2k/2M/25M	2k/2M/25M	2k/25M
Power Switch	-	-	-	-	-
LDO	-	-	-	-	-
DC/DC	-	-	-	-	-
Asynchronous State Machine	-	-	-	-	-
Temp Sensor	Yes	Yes	Yes (SLG46826)	Yes	Yes
Crystal Oscillator Cell	-	-	-	-	-
Communication Interface	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C
Package Size (mm)	2.0 x 3.0	2.0 x 3.0	2.0 x 3.0	3.0 x 3.0	1.6 x 1.6
Package Type	STQFN	STQFN	STQFN & TSSOP	STQFN	STQFN

# BACK UP SLIDES

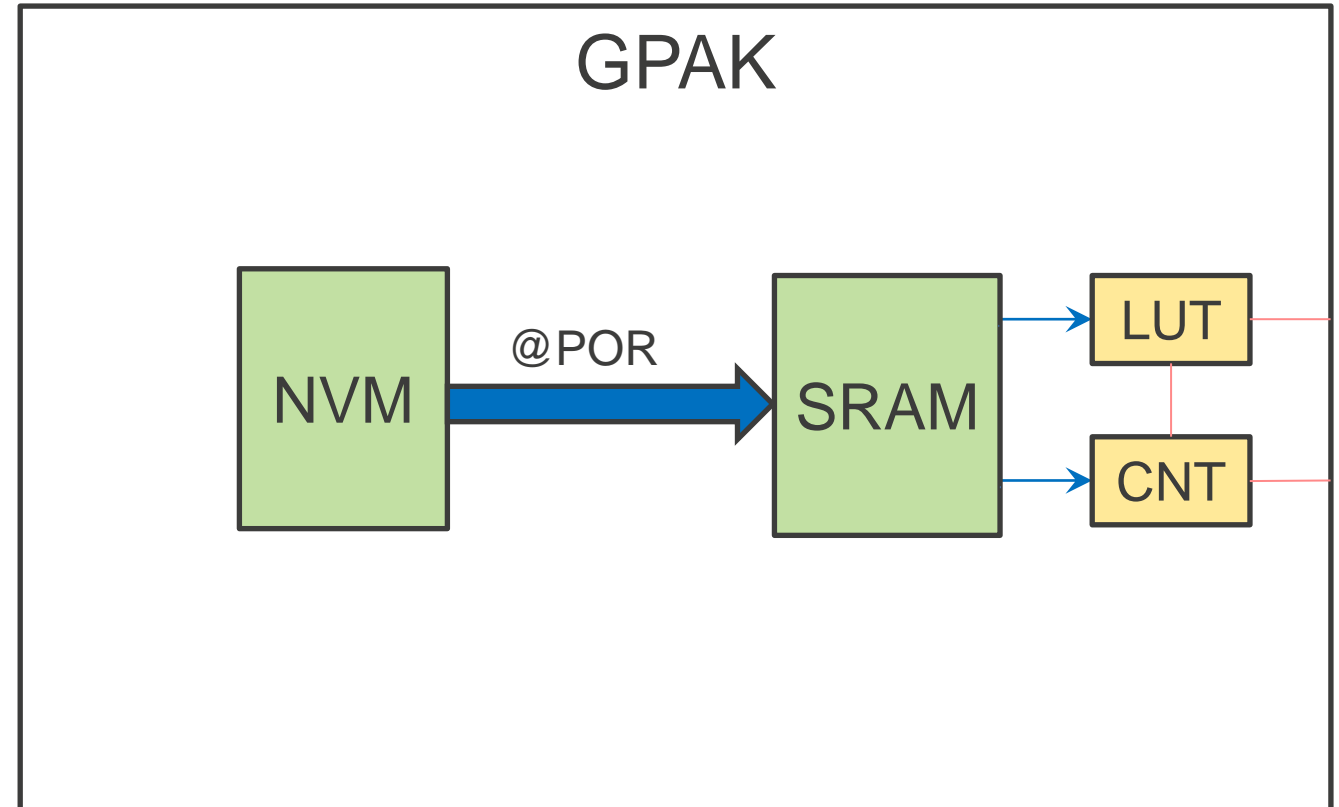
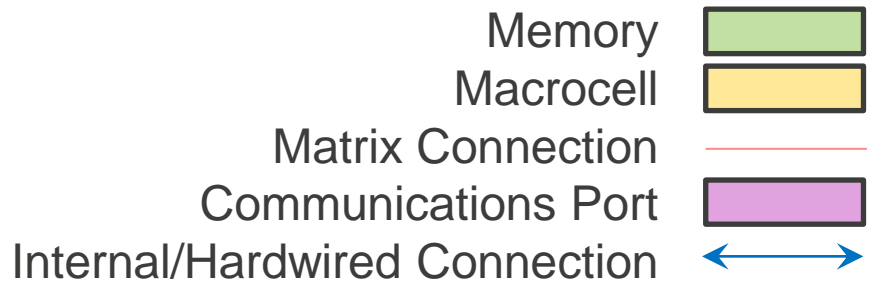
## GREENPAK POWER UP SEQUENCE



# GREENPAK – NO I2C BLOCK PRESENT

## Power Up Sequence

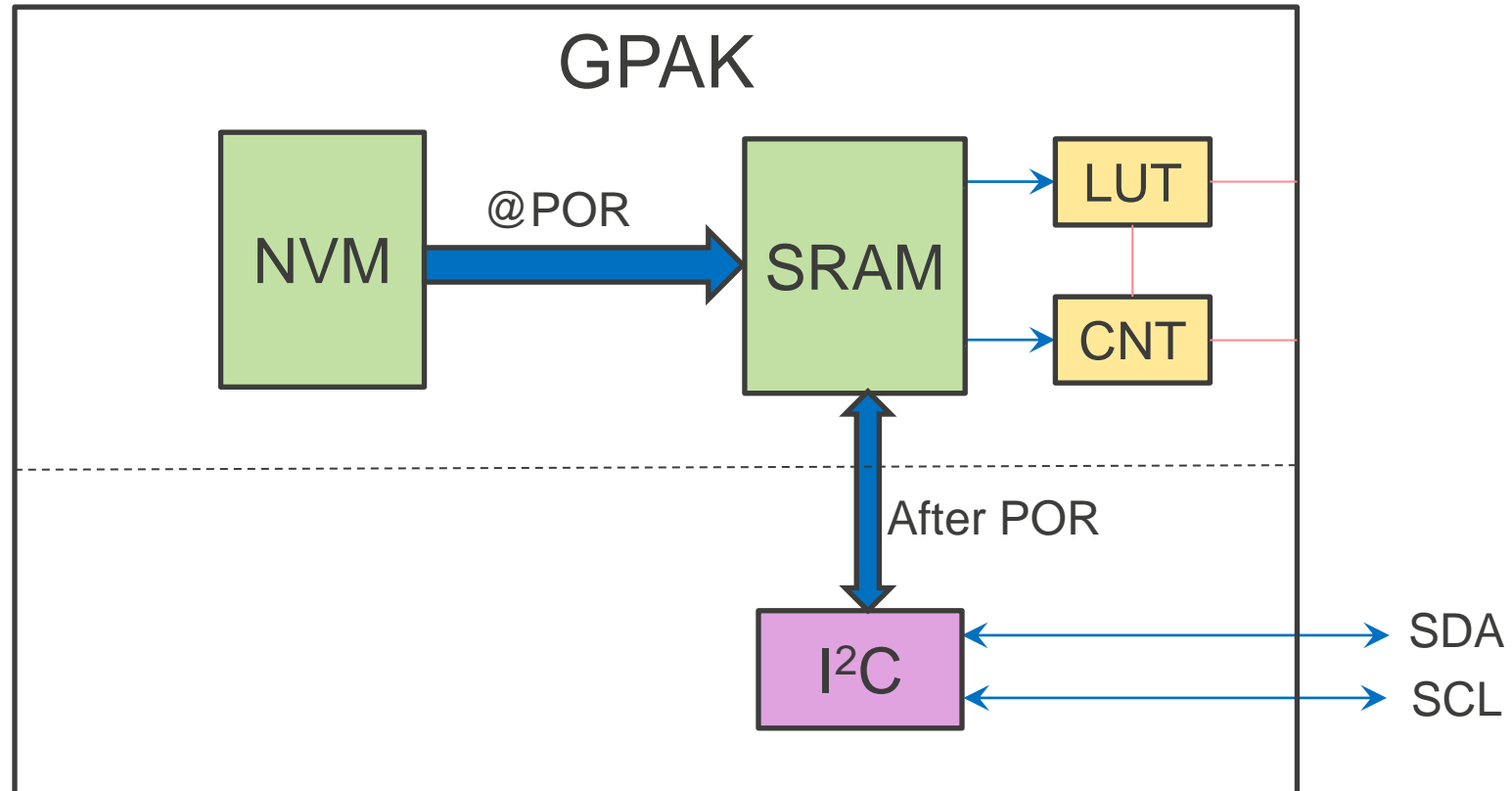
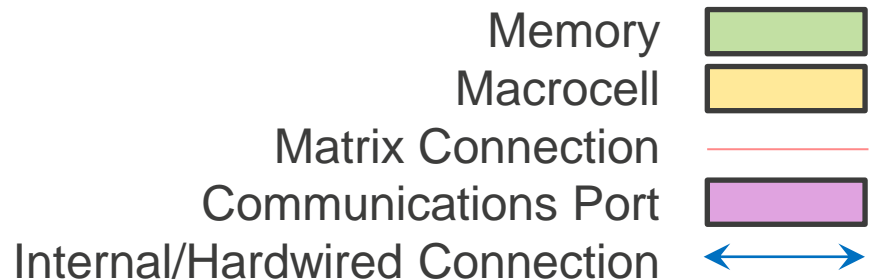
1. Apply VDD.
2. Internal POR goes active.
3. NVM copies to SRAM.
4. SRAM configures macrocells and matrix connections.



# GREENPAK – I2C BLOCK PRESENT

## Power Up Sequence

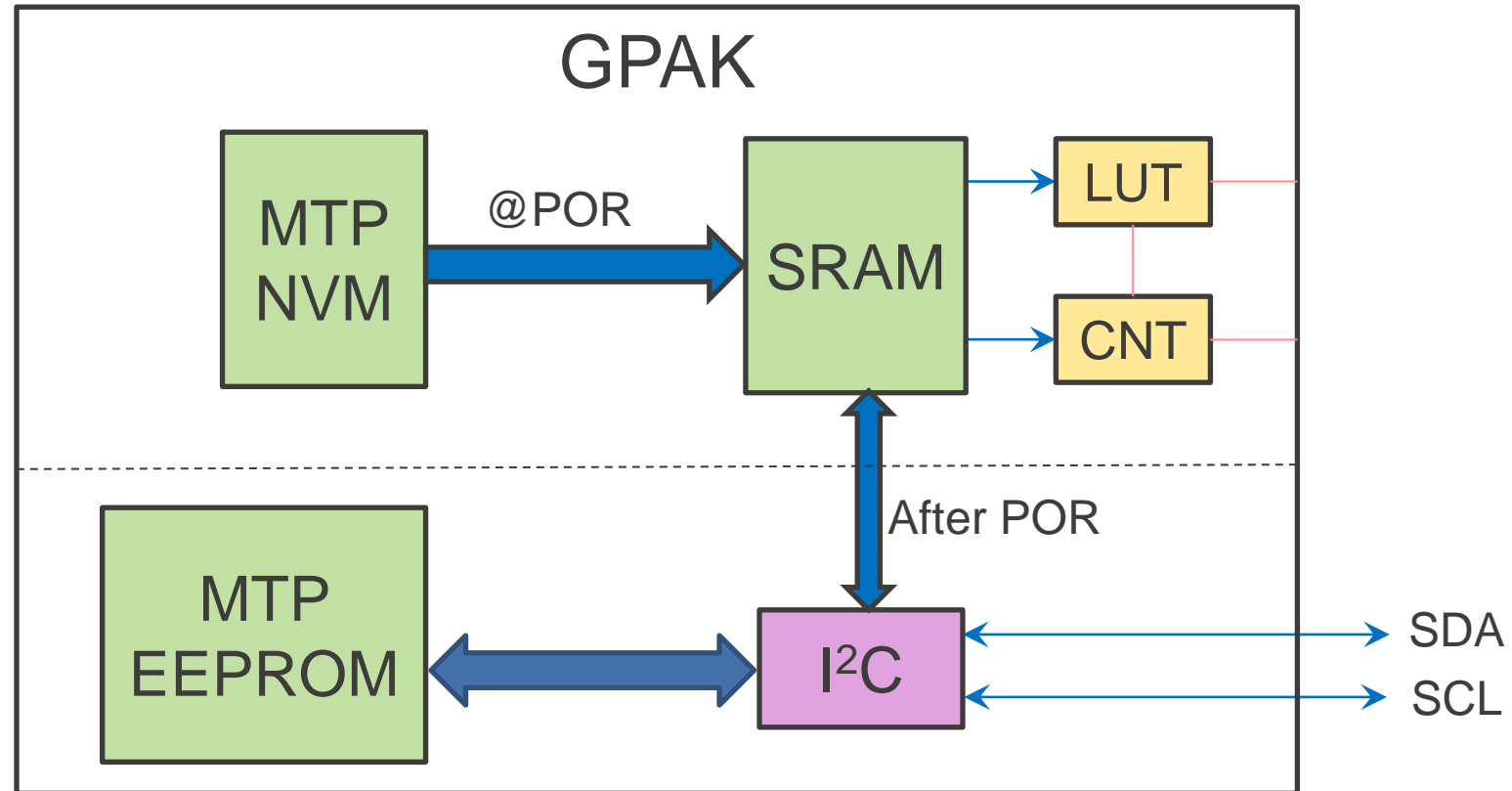
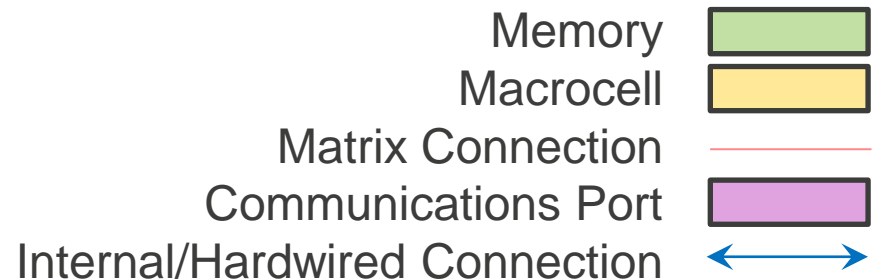
1. Apply VDD.
2. Internal POR goes active.
3. NVM copies to SRAM.
4. SRAM configures macrocells and matrix connections.
5. I2C can access SRAM to write changes. Changes are lost on POR or VDD cycle.



# GREENPAK – I2C BLOCK PRESENT AND IN SYSTEM PROGRAMMABLE

## Power Up Sequence

1. Apply VDD.
2. Internal POR goes active.
3. MTP NVM copies to SRAM.
4. SRAM configures macrocells and matrix connections.
5. I2C can access MTP NVM to write changes.
6. I2C can access MTP EEPROM which is independent of other chip blocks.



# BACK UP SLIDES

## AUTOMOTIVE GREENPAK

# GREENPAK™ PROGRAMMABLE MIXED-SIGNAL ASIC - SLG46XXX-A, SLG47XXX-A

## Value Proposition & Features

- Automotive grade, **AEC-Q100** compliant (Grade 2 available now, Grade 1 on the roadmap)
- Cost effective NVM programmable IC containing **digital and analog**
- Fewer parts = lower FIT, **less qualification & less sourcing** issues

### Solution Example

Infotainment/Cluster, xEV, MCS, ...



Power sequence, Voltage/Current/Temp detector, PWM, I/O expander, Button debounce/Glitch filter, Sensor AFE Watchdog, Reset control, Level shift/Buffer, Glue logic

### Benefit

- Automotive grade, AEC-Q100 compliant
- Combine multiple discrete ICs into one small package
- Small-scale custom IC without NRE, 18 weeks for MP
- GUI design tool available

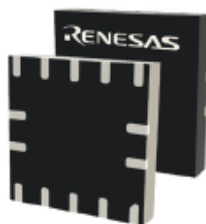


# ROADMAP FOR GREENPAK AEC-Q100 QUALIFICATION

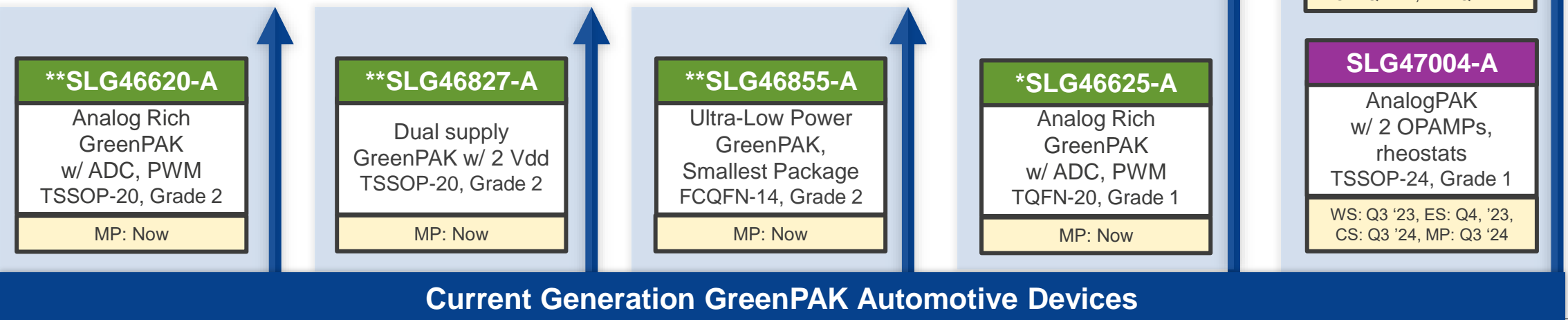
Scalable Solutions to Reduce Solution Size, Cost & Power



6.5 mm x 6.4 mm  
20-pin TSSOP  
0.65 mm pitch



3.0 mm x 3.0 mm  
14-pin FCQFN  
0.65 mm pitch



# GREENPAK AUTOMOTIVE PARTS

	SLG46620-A	SLG46827-A	SLG46855-A	SLG46625-A
Status	Production	Production	Production	Sampling
# of GPIOs	20/18	20/17	14/12	20/18
Operating Voltage (V)	1.71 to 3.6	2.3 to 5.5	2.3 to 5.5	1.71 to 5.0
Dual Supply		1.71 to Vdd	-	-
In-System Debug	No	Yes	No	No
8-bit SAR ADC	1	-	-	1
Analog/Digital Comparators	6/3	4/0	4/0	6/3
Look Up Tables (LUTs)	25	0	0	25
Combinational Function Macro-cells	1 Total	11 Total	15 Total	1 Total
Multifunction Macrocells	0	8	8	0
PWMs	3	-	-	3
Counter/Delays	10	-	-	10
DFF/Latch	12	-	-	12
Pipe Delay	2 x 16-stage	16-stage	16-stage	2 x 16-stage
Programmable Delay	2	1	1	2
Internal Oscillator (Hz)	1.7 k/25 k/2 M/27 M	2 k/2 M/25 M	2 k/2 M/25 M	1.7 k/25 k/2 M/27 M
Load Switch	-	-	-	-
LDO	-	-	-	-
Asynchronous State Machine	-	-	-	-
Communication Interface	SPI	I <sup>2</sup> C	I <sup>2</sup> C	SPI
Package	6.4 mm x 6.5 mm TSSOP-20	6.4 mm x 6.5 mm TSSOP-20	3.0 mm x 3.0 mm FCQFN -14	3.5 mm x 3.5 mm TQFN-20
Package Pitch	0.65	0.65	0.65	0.5
Temperature Grade	2	2	2	1

# GREENPAK AUTOMOTIVE PARTS

	SLG46857-A	SLG46880-A	SLG46538-A	SLG47004-A
Status	Sampling	Sampling	Sampling	Sampling
# of GPIOs	14/12	32/28	20/17	24/20
Operating Voltage (V)	2.3 to 5.5	2.3 to 5.5	1.71 to 5.5	2.4 to 5.5
Dual Supply	-	2.3 to VDD	1.71 to 5.5	-
In-System Debug	No	No	No	Yes
8-bit SAR ADC	-	-	-	-
Analog/Digital Comparators	4/0	5/0	4/0	3/0
Look Up Tables (LUTs)	0	-	-	0
Combinational Function Macro-cells	15 Total	12 Total	17 Total	13 Total
Multifunction Macrocells	8	0	0	7
PWMs	-	-	-	-
Counter/Delays	-	-	-	-
DFF/Latch	-	-	-	-
Pipe Delay	16-stage	16-stage	16-stage	16-stage
Programmable Delay	1	1	1	1
Internal Oscillator (Hz)	2 k/2 M/25 M	2 k/2 M/25 M	25 k/2 M/25 M	2 k/2 M/25 M
Load Switch	-	-	-	-
LDO	-	-	-	-
Asynchronous State Machine	-	12-state	8-state	-
Communication Interface	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C	I <sup>2</sup> C
Package	3.0 mm x 3.0 mm FCQFN -14	5.0 mm x 5.0 mm TQFN - 32	3.5 mm x 3.5 mm TQFN-20	4.0 mm x 4.0 mm TSSOP-24
Package Pitch	0.65	0.5	0.5	0.5
Temperature Grade	1	1	1	1



# RENESAS MANUFACTURING ADVANTAGES

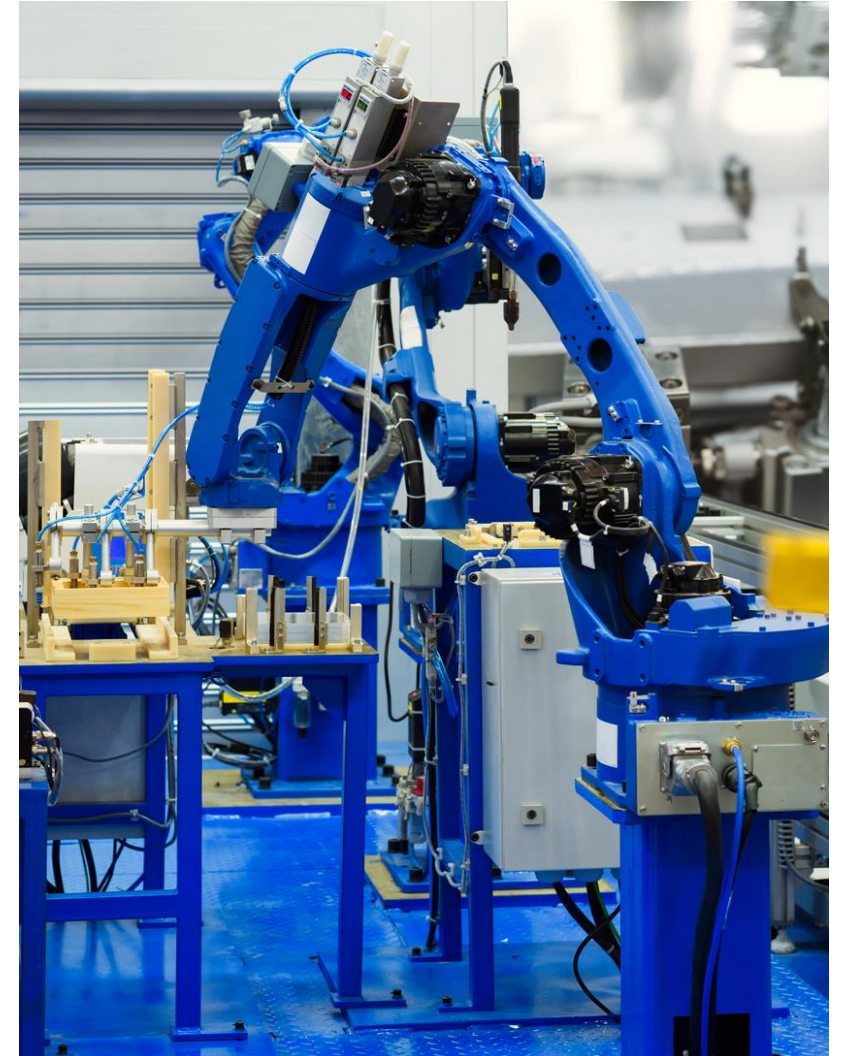
---

## Device Level Features

- **Ambient Operating Temperature Range:** -40 °C to 105 °C (grade 2) or -40 °C to 125 °C (grade 1)
- **Moisture Sensitivity Level:** 1 (Unlimited)
- **ESD Protection:** 2 kV HBM, 500+ V CDM
- **Quality Management:** ISO9001:2010 certified, AEC-Q100 qualified
- **Failure Rate:** < 10 DPPM
- **Long Product Lifecycles:** Driven by customer requirements
- **Environmental:** All subcons ISO14001, RoHS Compliant , Halogen-Free

## Design Benefits

- Higher Reliability
- Design Security
- Tested Solution



# DESIGN PORTION OF DEMO

USING GREENPAK DESIGNER (PART OF GO CONFIGURE SOFTWARE HUB)

CREATING A SIMPLE RESET CIRCUIT

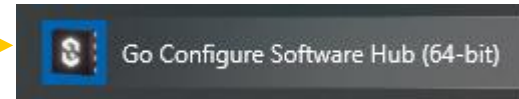
# STARTING THE PROCESS

## Launch GreenPAK Designer

- After you have installed [GoConfigure Software Hub](#), open up the program
- Click the Windows button in the bottom left corner of your screen
- Scroll to the GoConfigure Software Hub icon and click once to open it
- Click the GoConfigure Software Hub

- The first time you launch GoConfigure Software Hub, you will land on the Welcome page. Click the “Develop” page next.

- This will give you a window that shows the selection of GreenPAK parts available
- Single click the SLG46826V to highlight it
- Double click on SLG46826V to launch the designer for this silicon



The screenshot shows the GoConfigure Software Hub interface. The top navigation bar includes 'Welcome', 'Develop', and 'Demo'. The main content area displays a table of GreenPAK parts. The SLG46826V part is highlighted in blue. Below the table, there is a 'Details' section for the selected part, including package information, supported development platforms, and a description of the device's features and capabilities.

Part Number	DS	VDD (V)	VDD2 (V)	GPIO	AEC-Q100	Special Features	ACMP	DCMP	Max. CNT/DLY	Max. LUT	Max. DFF
SLG51000C	<a href="#">Contact us</a>	2.8 to 5.0	-	6	-	-	-	-	-	12	-
SLG31001C	<a href="#">Contact us</a>	2.8 to 5.0	-	4	-	-	-	-	-	12	-
SLG47910V	<a href="#">Contact us</a>	0.99 to 1.21	1.71 to 3.6	19 + PWR, EN	-	Dense Logic Array; PLL; BRAM	-	-	-	-	-
SLG51002C	<a href="#">Contact us</a>	2.8 to 5.0	1.2 to 5.0	8	-	-	-	-	-	8	-
SLG47004V	<a href="#">DS</a>	2.4 to 5.5	-	8	-	2x Op Amp or 1x In-Amp; 2x Rheostat; 2x An. Switch; 2-Ch Auto-Trim; EEPROM	3	-	7	20	1
SLG47115V	<a href="#">DS</a>	2.3 to 5.5	4.5 to 26.4	8 + 2x HD	-	1x H/2x Half-Bridge; 2x PWM; COMP; IntSDiff Amp	2	-	5	17	1
SLG47105V	<a href="#">DS</a>	2.3 to 5.5	3.0 to 13.2	8 + 4x HD	-	2x H/4x Half-Bridge; 2x PWM; 2x COMP; IntSDiff Amp	2	-	5	17	1
SLG46811V	<a href="#">DS</a>	2.3 to 5.5	-	10	-	92 x 8 bit Pattern Generator	1 (4)	-	6	18	1
SLG47513M	<a href="#">DS</a>	1.0 to 1.65	-	14	-	-	2	-	8	23	2
SLG47512V	<a href="#">DS</a>	1.0 to 1.65	-	10	-	-	2	-	8	23	2
SLG46826V	<a href="#">DS</a>	2.3 to 5.5	-	10	-	2x P-FET (44mΩ, 2A)	4	-	8	23	2
SLG46857-AP	<a href="#">Contact us</a>	2.3 to 5.5	-	12	Grade 1	-	4	-	8	23	2
SLG46855-AP	<a href="#">Contact us</a>	2.3 to 5.5	-	12	Grade 2	-	4	-	8	23	2
SLG46855V	<a href="#">DS</a>	2.3 to 5.5	-	12	-	-	4	-	8	23	2
SLG46827-AG	<a href="#">DS</a>	2.3 to 5.5	1.71 to VDD	17	Grade 2	-	4	-	8	19	1
SLG46836G	<a href="#">DS</a>	2.3 to 5.5	1.71 to VDD	17	-	-	4	-	8	19	1
SLG46826V	<a href="#">DS</a>	2.3 to 5.5	1.71 to VDD	17	-	-	4	-	8	19	1

# SETTING UP PROJECT INFO

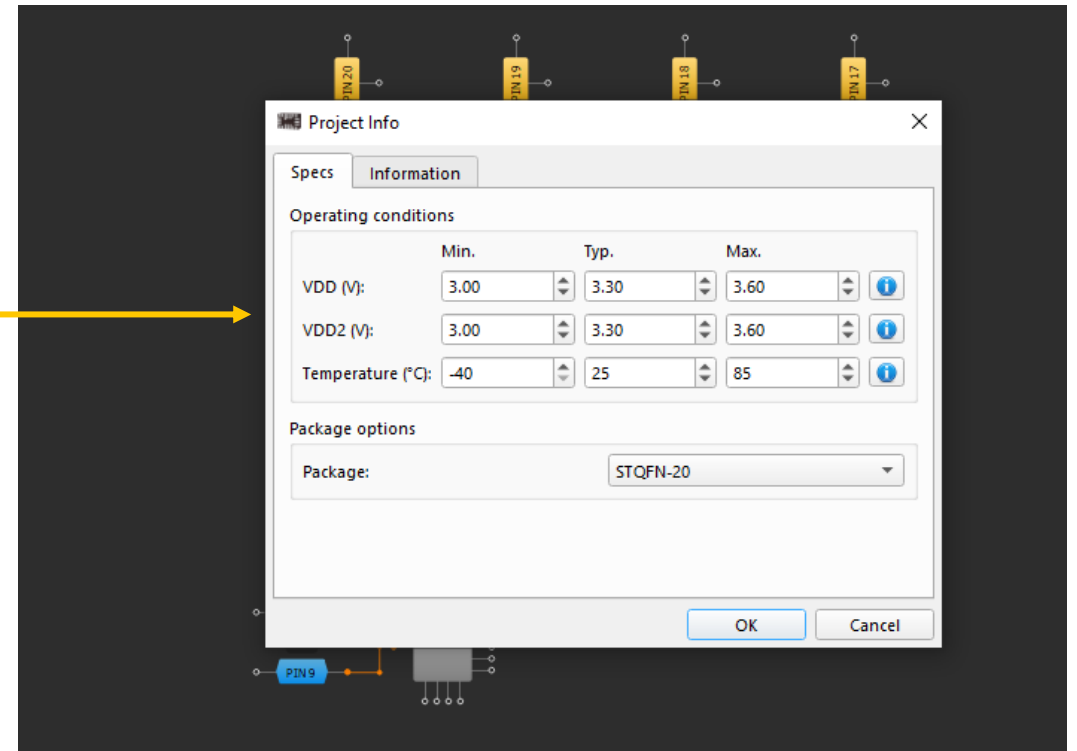
## Entering VDD, VDD2 and Temperature Information

- You will get a window with “Project Info” that opens automatically

- Set:

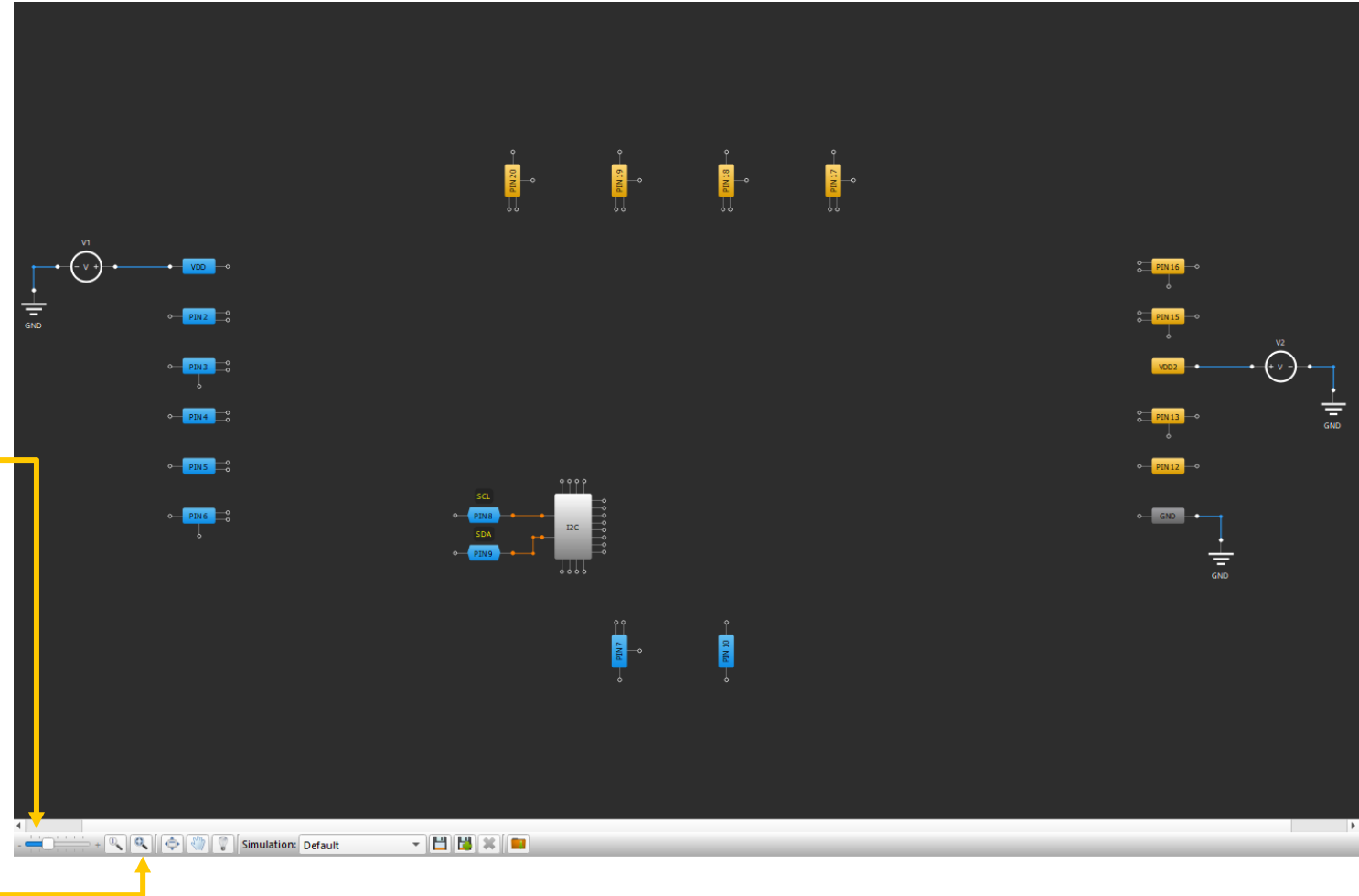
- VDD to 3.0, 3.3, 3.6
- VDD2 to 3.0, 3.3, 3.6
- Temp to -40, 25, 85

- This information will be used when we want to test or simulate the design



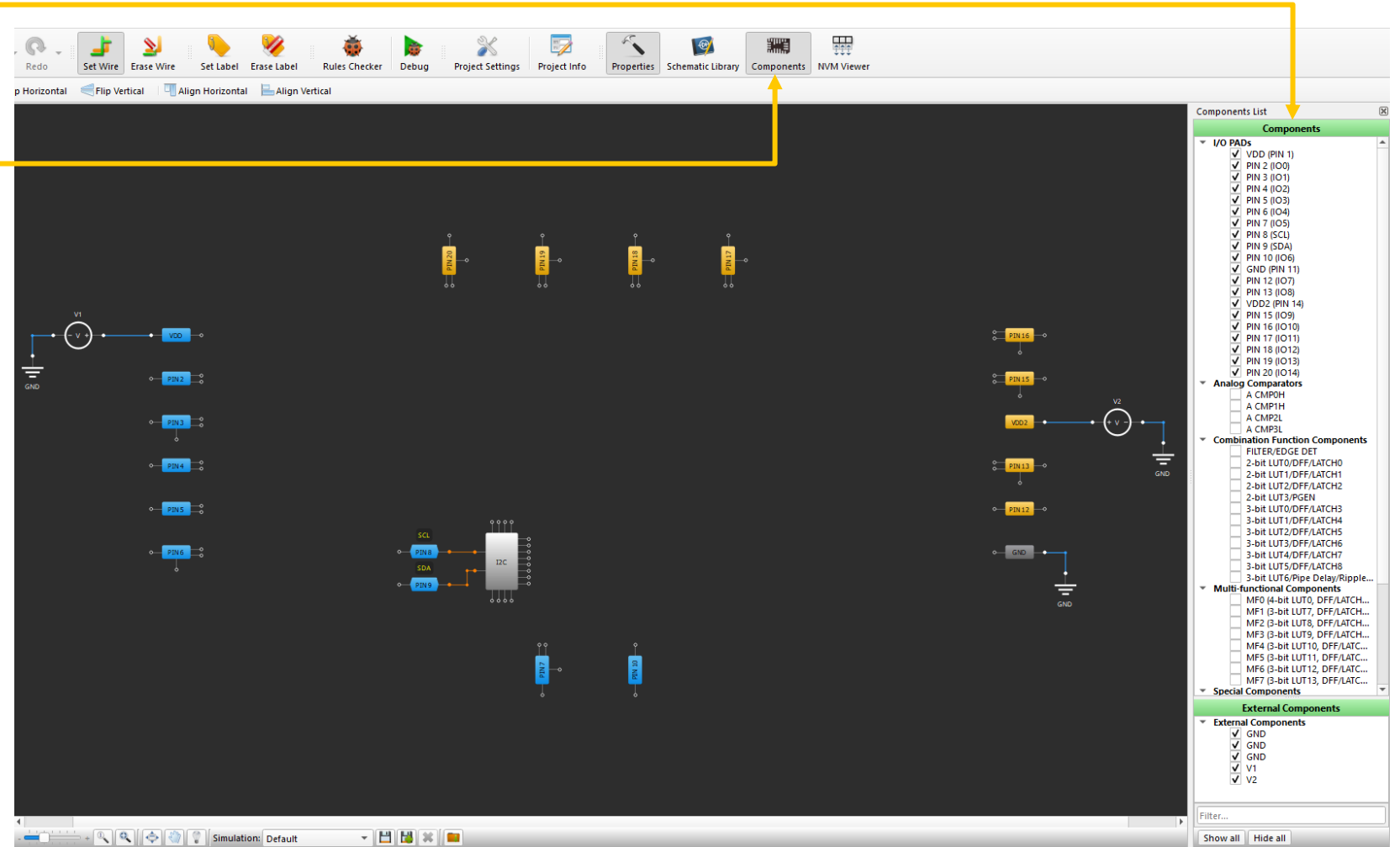
# RESIZING MAIN WINDOW

- Use slider bar here to adjust view to show all pins (should look like this when you are done)
- Alternatively, you can select the “Fit Work Area” button to auto scale the view
- Pins shown have two types:
  - Blue pins connected to VDD
  - Gold pins connected to VDD2
  - These are available on all dual-supply parts



# COMPONENTS WINDOW

- Components list should be shown on right hand side
- If it is not showing, click on Components button to make it show
- The components window shows the available circuit components
- The components in each base device are different, therefore the components window is unique for each device type



# OUR GOAL IS TO DESIGN A SIMPLE RESET CIRCUIT

---

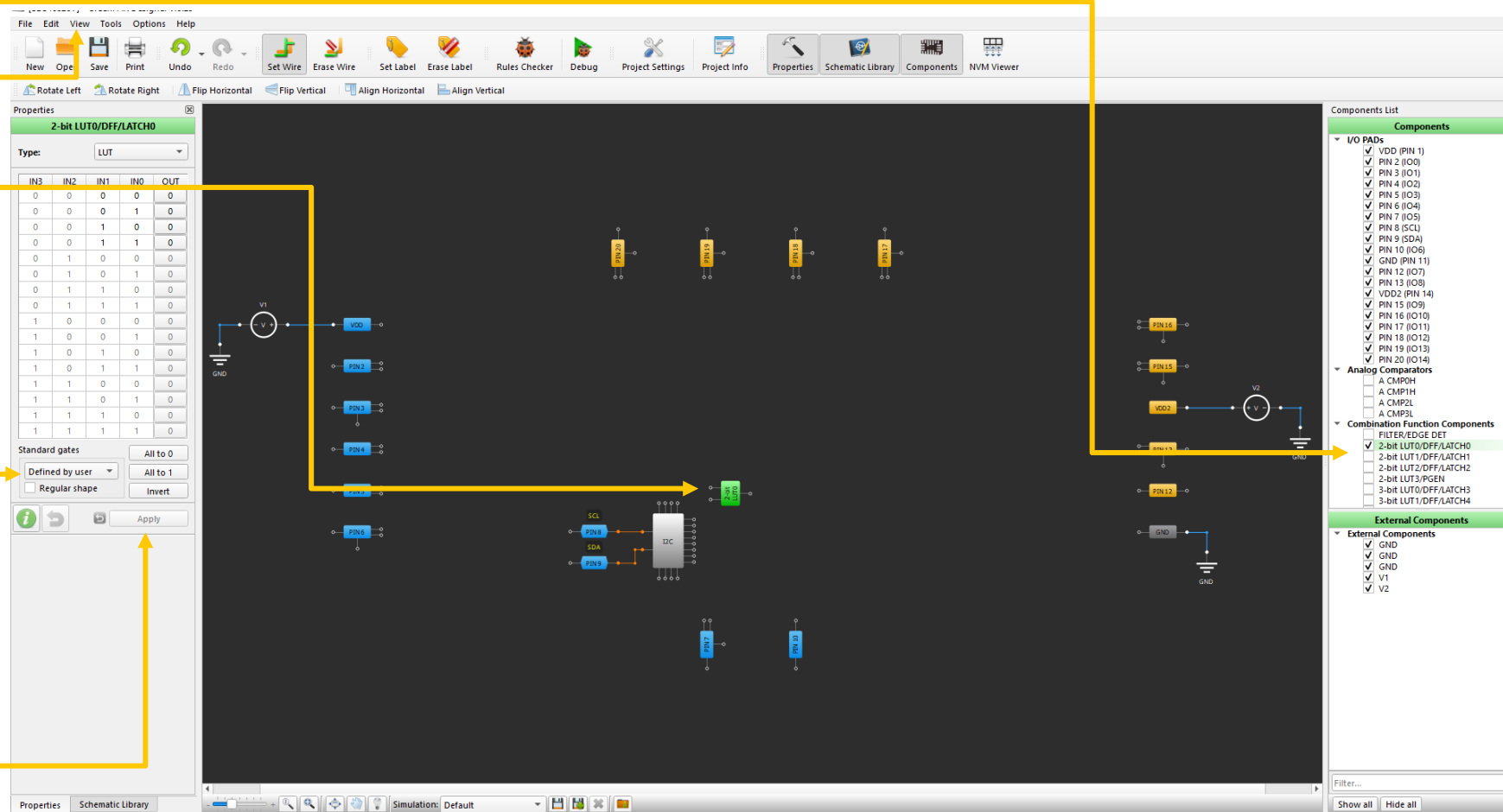
## Three Functions in the Design

- This design will issue an output pulse that can trigger a reset of a system
- This function has three components in this example:
  - Logic “OR” gate
  - Analog comparator (ACMP)
  - One shot (pulse generator)
- Let’s review what each component does in this example:
  - One shot – this is the output pulse that a monitoring device will use to reset the system
  - ACMP – this will monitor a voltage rail (for example a main power rail)
  - “OR” gate – this will be used to monitor two possible signals that can trigger a reset
    - ACMP output for the case where the power rail goes too low
    - Digital logic input for the case where another device wants to trigger a reset
- The signal flow looks like this: digital logic “OR” ACMP → One shot

# SELECTING A COMPONENT (LOGIC GATE)

## Configuring the Gate

- Click on 2-bit LUT0
  - Check the box next to the name of the block
- Make sure the block is highlighted green
- If it's not, click the item once
- Click "View" "Properties" if necessary
- Set the logic block to be an "OR" gate
  - From the drop-down menu, select "OR"
- Click "Apply" to keep the changes

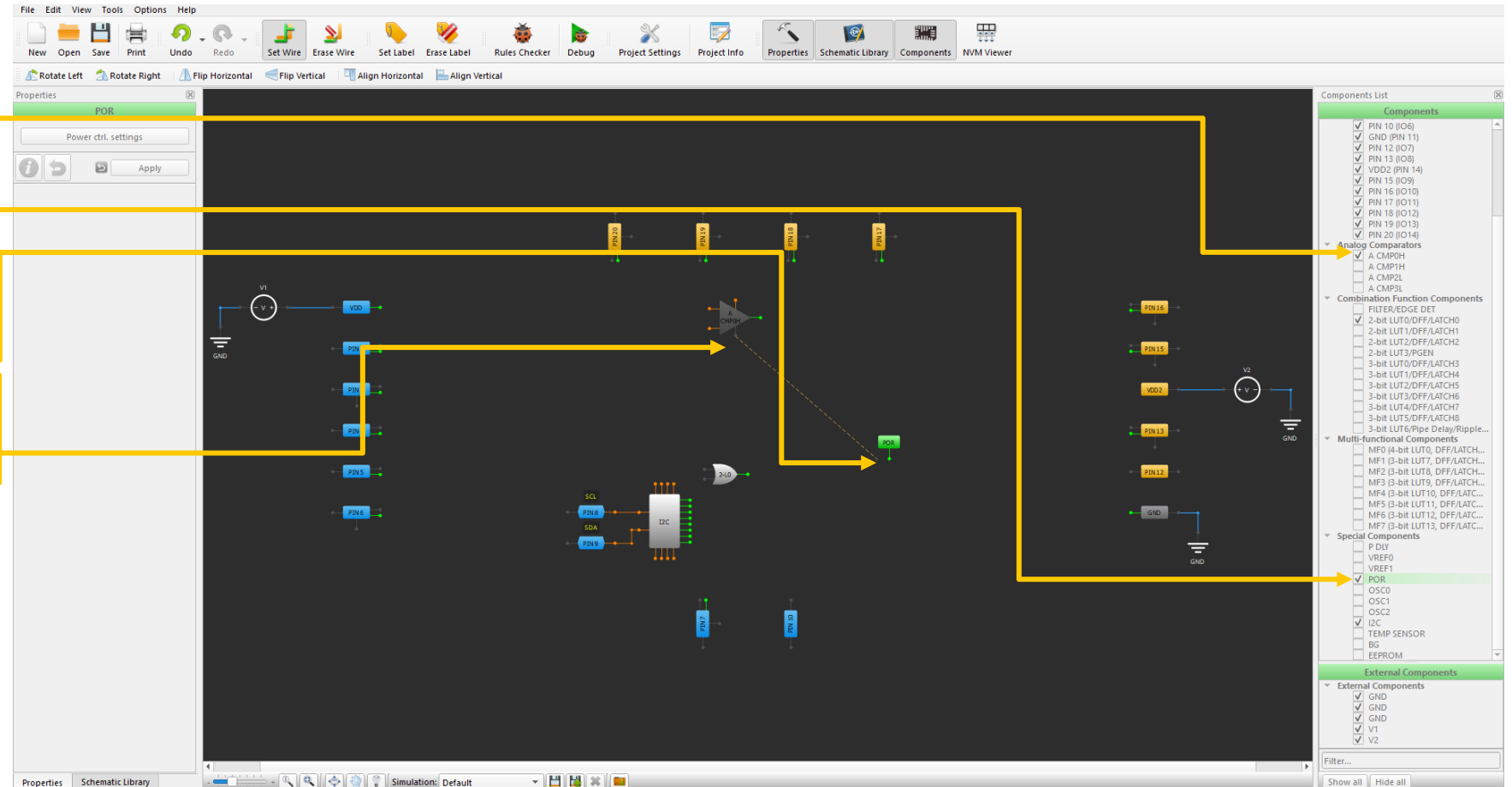




# SELECTING A COMPONENT (ANALOG COMPARATOR)

## Configuring the ACMP

- Click on ACMP0H
  - Check the box next to the name of the block
- Click on POR
- Click the pin of POR so that you start a “wire” connection
- Connect the wire to the “power” pin of the ACMP
- This powers the ACMP whenever the POR is on
- Pin 20 will default to an analog input and connect to IN+ of the ACMP



# SELECTING A COMPONENT (ONE SHOT)

## Configuring the Counter Block as a One Shot

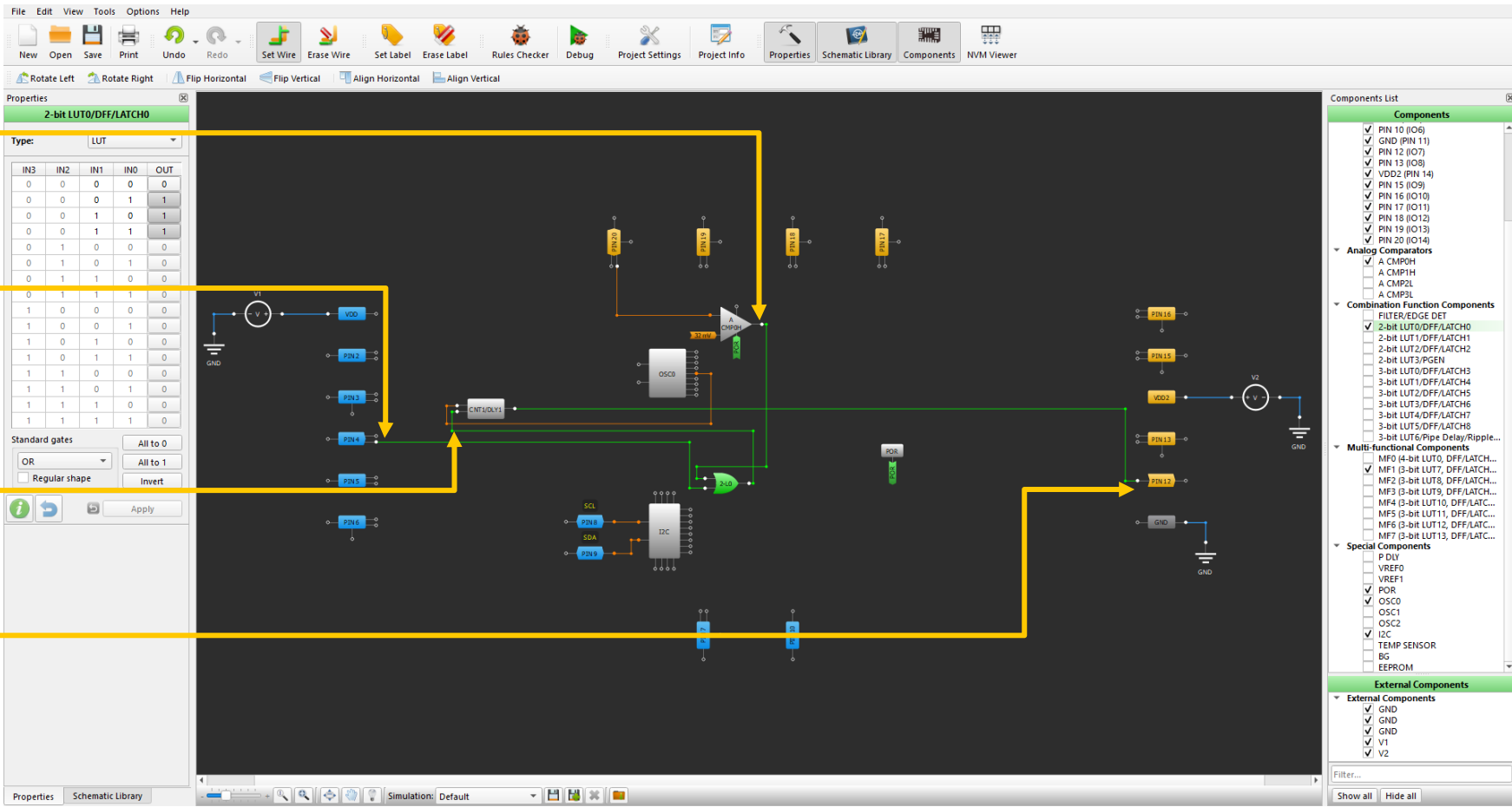
- Click on MF1 block
  - MF = Multi-Function
- Use the drop-down menu to change it to a counter
- Click “Apply” and “Yes”
- Use 2<sup>nd</sup> drop-down menu and change to One Shot
- Click “Apply”
- Select OSC0/64 from the drop-down menu for oscillator
- Click “Apply”
- OSC0 appears with an orange wire to CNT1

The screenshot displays the Renesas IDE interface for configuring a component. The Properties panel on the left is titled "8-bit CNT1/DLY1 (MF1)". It features a "Multi-function mode" dropdown menu set to "CNT/DLY", a "Mode" dropdown menu set to "One shot", and various configuration options for counter data, pulse width, edge select, and output polarity. The Connections panel shows the "Clock" dropdown menu set to "OSC0/64", with "Clock source" set to "OSC0 Freq./64" and "Clock frequency" set to "32 Hz". The Schematic Library panel shows the "8-bit CNT1/DLY1" component selected. The Components List on the right shows the "Multi-functional Components" section with "MF1 (3-bit LUT7, DFF/LATCH...)" selected. The Schematic Editor shows the circuit diagram with the 8-bit CNT1/DLY1 block connected to the OSC0/64 oscillator and the output connected to the V2 pin.

# CONNECTING BLOCKS TOGETHER

## Using Wires

- Use a wire to connect ACMP output to IN1 of "OR" gate
- Wire Pin 4 output to IN0 of "OR" gate
- Wire "OR" gate output to CNT1 "DLY IN"
- Wire CNT1 one shot output to Pin 12



# WHAT DOES THIS DESIGN DO SO FAR?

---

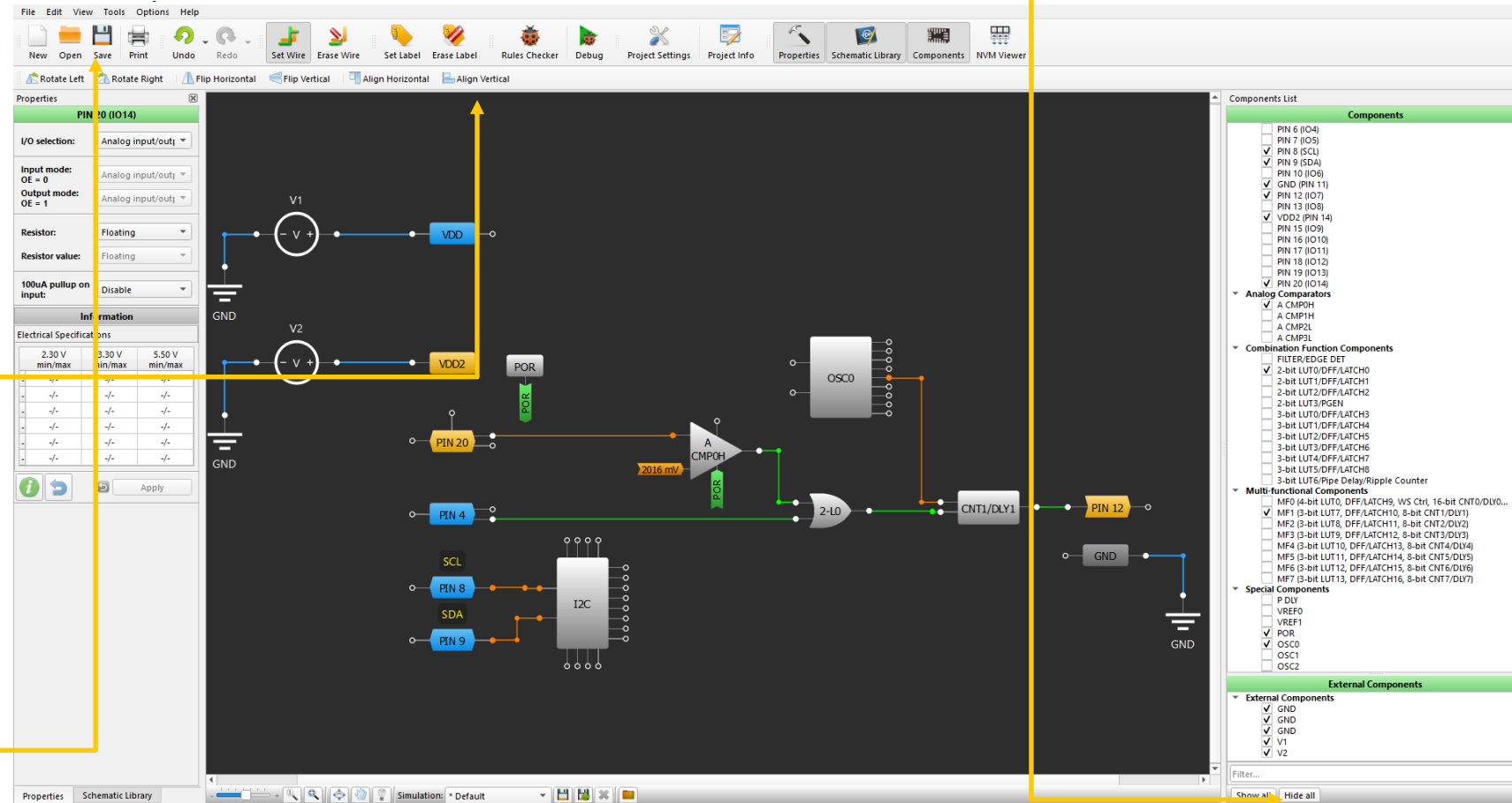
## Design Operation

- If Pin 4 goes to a logic high, OR Pin 20 goes above the ACMP VREF (currently defaulted to 32 mV), then the output of the OR gate will go HI.
- Upon a HI or LO from the OR gate the CNT1 one shot trigger. The one shot pulse is currently set to be a 62.5 msec, HI pulse (output polarity = not inverted).
- Let's say that Pin 20 is tied to the VDD of an S.O.C. When the SOC VDD goes HI, the output of the OR gate will go HI, triggering the one shot output pulse. Since an SOC takes some time to power up, we might cause a reset of the SOC mid-power up. We can fix this by changing the CNT1 edge to "Falling".
- Also, 32 mV might be a little low to compare the VDD value to so let's change that to 2016 mV (2.016 mV). This is now configured as a much better "brownout" detector.

# CLEANING UP THE LAYOUT

## Rearrange and Remove Unused Pins

- To remove unused pins, click “Hide All”.
- To move blocks around, click and hold a block to drag them around the screen. This is shown by a hand-shaped cursor.
- To align pins vertically, drag a highlighted box around Pins 4, 8, 9 and 20. Then click the “Align Vertical” button.
- To rotate a block, click it once, then right click and rotate it.
- Save early, save often!



# SIMULATION PORTION OF DEMO

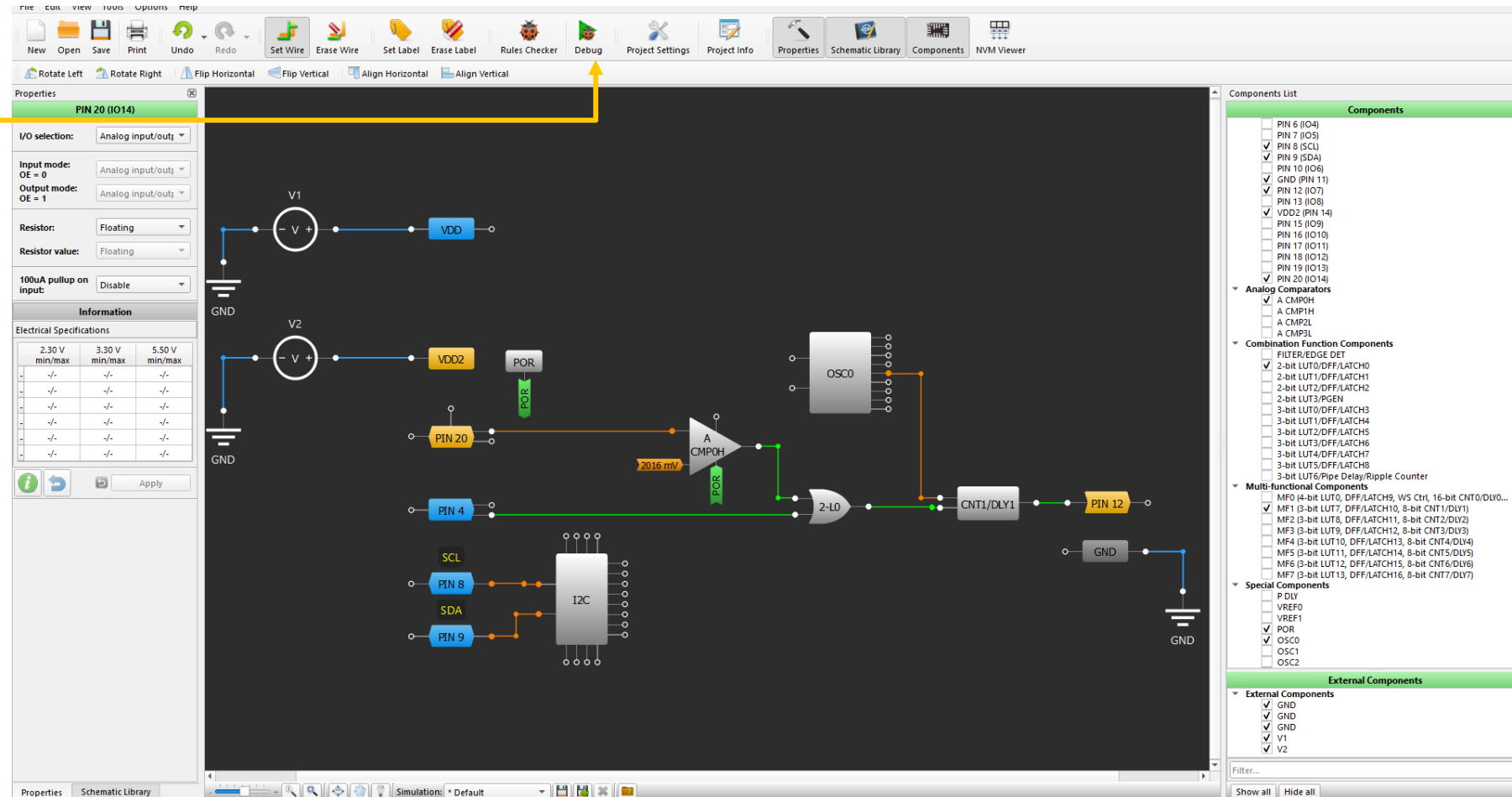


# OPEN THE DEBUGGER

## This is How to Access the Built-In Simulator (SPICE)

- Click the “Debug” button to access the SPICE simulator

- This is also how to access the emulator for the various hardware development kits



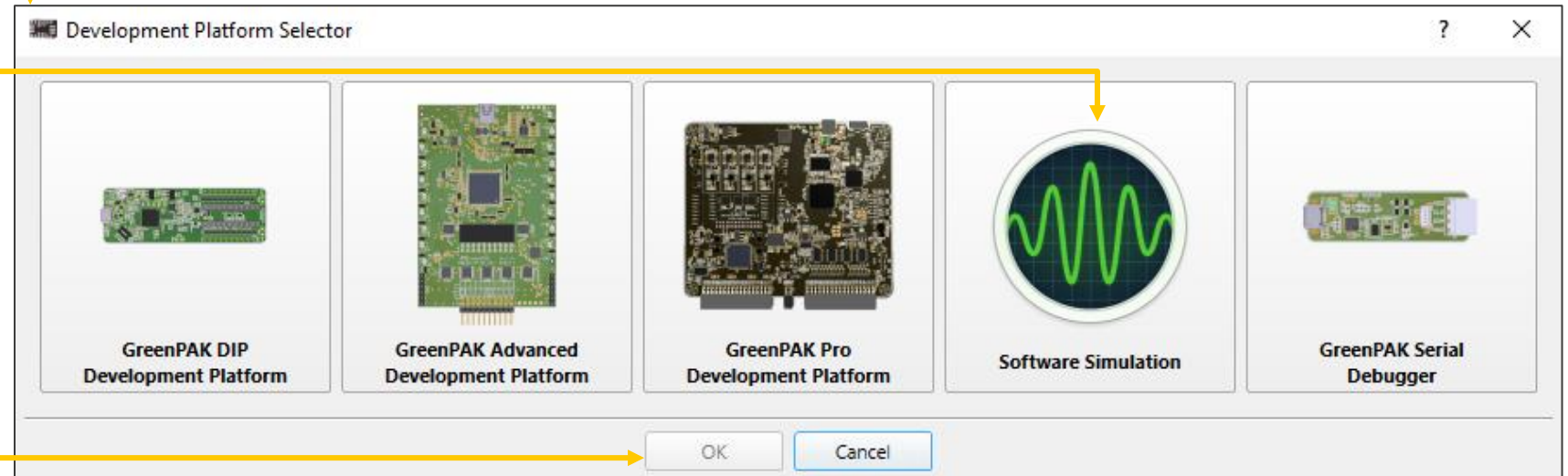
# DEVELOPMENT PLATFORM SELECTOR WINDOW

## Accessing the SPICE Software Simulation Tool

- The Development Platform Selector window should be visible

- We want to use the Software Simulator to test the design, so select it

- Click OK

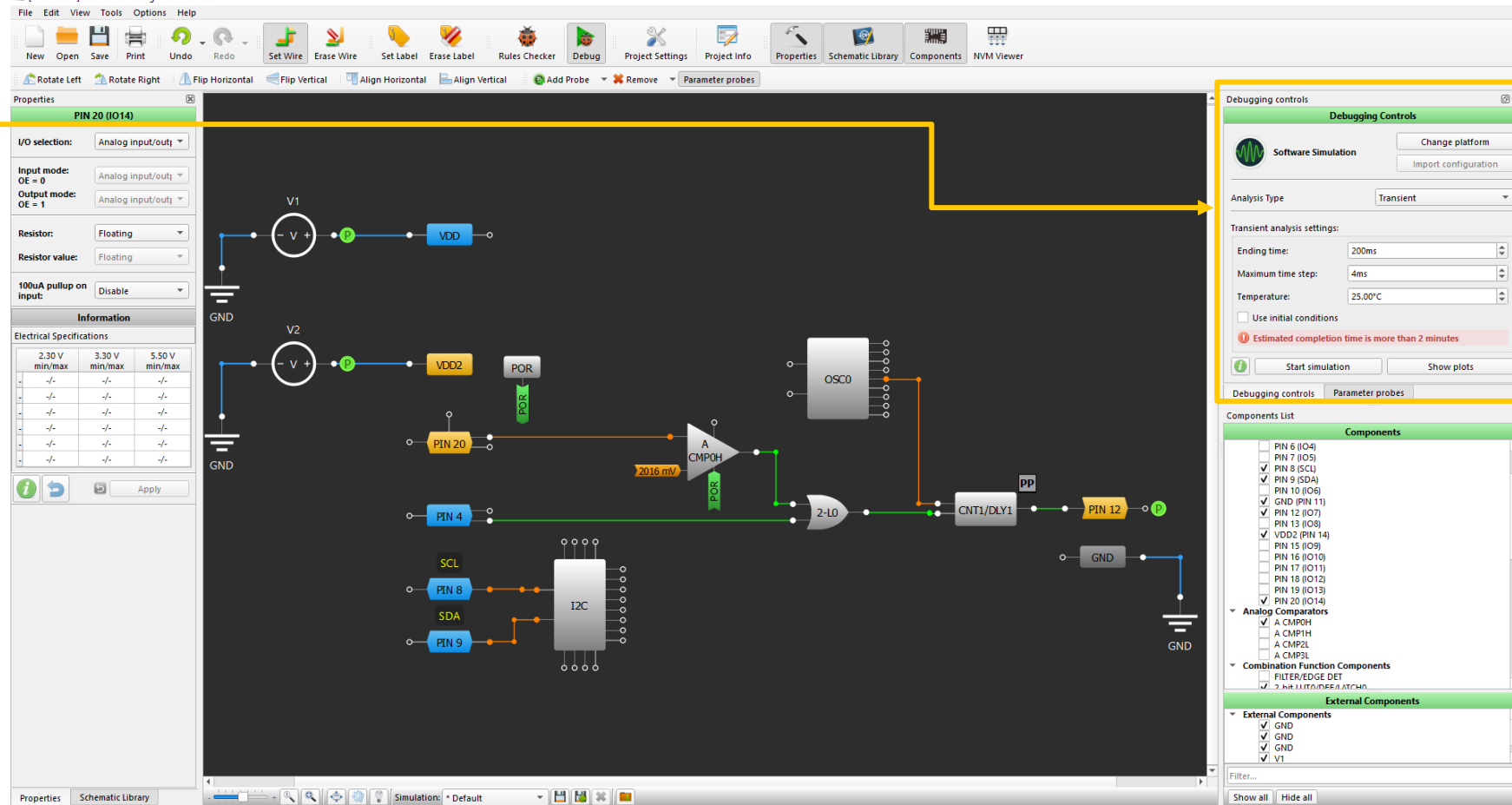




# THE DEBUGGER CONTROLS WINDOW

## Setting Simulation Parameters

- This window allows you to define the parameters of the simulation run
- Before we run the simulation, we need to set input signals and choose probe points (circuit connection points where the simulation software will track the outputs)



# ADD VOLTAGE SOURCE AND PROBE POINT

For Both Input Pins and the Output Pin

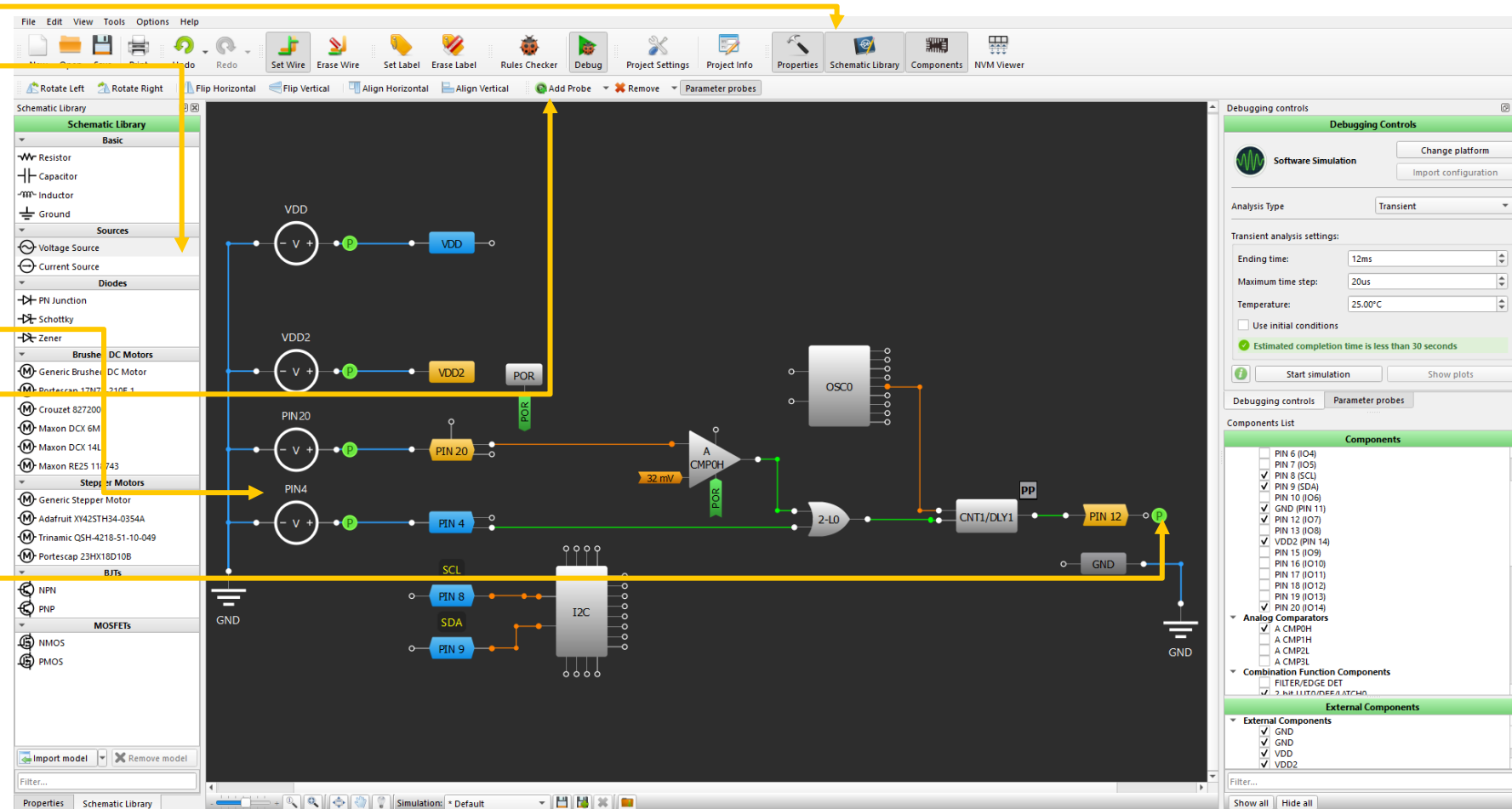
- Click „Schematic Library”, then “Voltage Source”

- Add voltage sources to VDD, VDD2, Pin 4, and Pin 20

- Click “Add Probe”

- Click the external connection for Pin 12

- Green probe appears



# EDIT AND CONFIGURE THE SOURCE

## Setting Source Simulation Parameters

- Double click the source for Pin 20
- You should see this window pop-up
- Note that we are looking at the source for Pin 20
- Change its type to sine
- Change the amplitude to 2.8 V
- Change the frequency to 5 Hz
- Click "Apply"
- Close the window

The image shows a 'Source Setup' dialog box with two tabs: 'General' and 'Voltage Source Settings'. The 'General' tab is active, showing 'Source: PIN20', 'Name: PIN20', 'Pre-start delay: 0.000 ms', and checkboxes for 'Show only one period' (unchecked), 'Limit voltage to VDD and GND level' (checked), and 'Customize source' (unchecked). The 'Voltage Source Settings' tab is also visible, showing 'Type: Sine', 'Zero offset: 1.000 V', 'Amplitude: 2.800 V', 'Frequency: 5.000 Hz', and 'Damping factor: 0.000 Hz'. The 'Apply' button is highlighted at the bottom. To the right, four simulation waveforms are shown: VDD (constant at 3.3V), VDD2 (constant at 3.0V), PIN20 (a sine wave between 1.0V and 3.8V), and PIN4 (constant at 3.3V). The x-axis for all waveforms is time in milliseconds, ranging from 0.00 to 200.00.

# SET AND RUN THE SIMULATION

- Change the Ending Time to 200 ms

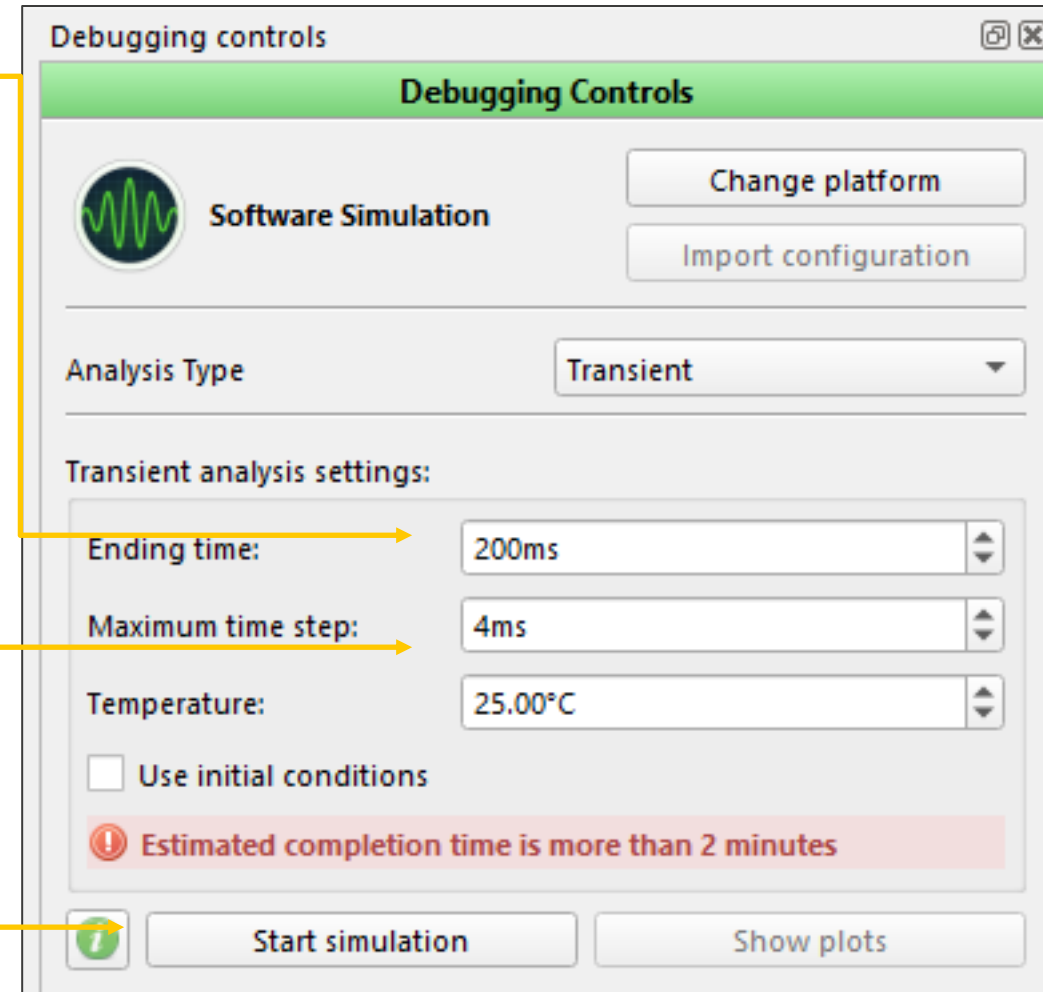
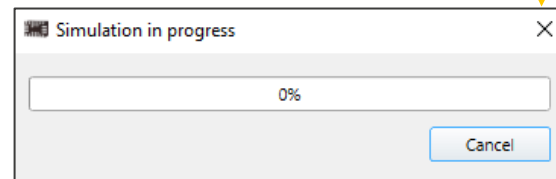
- Change the Maximum time step to 4 ms

- Note that the default is in  $\mu\text{s}$

- Push this button to start the simulation

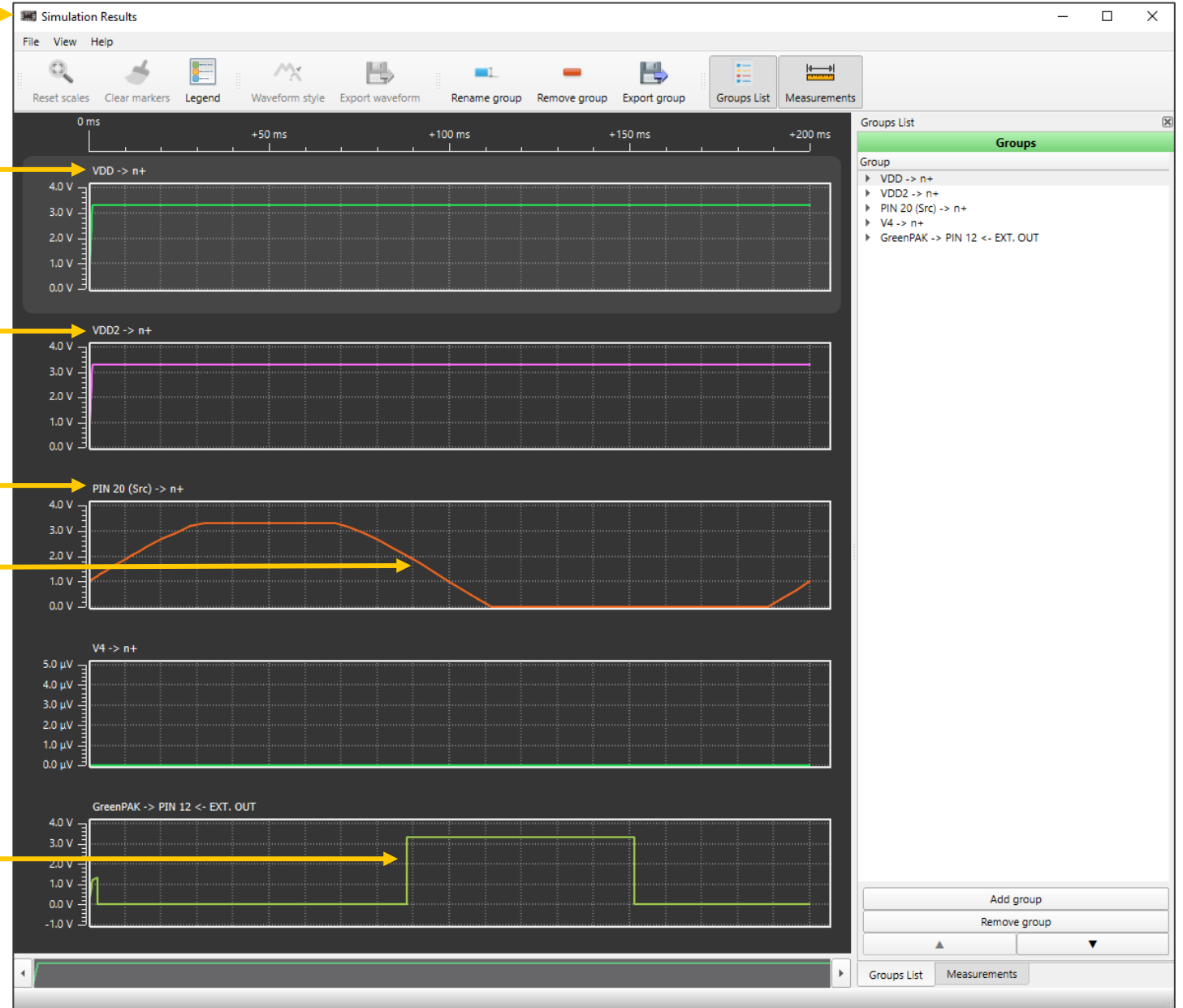
- A warning pop-up may appear to show a long simulation time, it's ok to dismiss

- This pop-up window shows the progress



# SIMULATION RESULTS

- Results show in a new window
- VDD voltage for 200 ms
- VDD2
- Input voltage on Pin 20
- Since the one shot trigger was set to falling edge, as the sine wave input falls below 2.016 V, we will cause the one shot pulse to be output
- Note the pulse width is 62.5 ms as designed



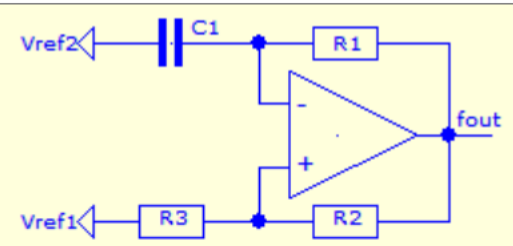
# BACK UP SLIDES ADDITIONAL APPLICATIONS EXAMPLES

# GREENPAK APPLICATION EXAMPLES

## Multivibrator (Op Amp Design)

- Uses the OPAMP0 in SLG47004V
- As there is no negative Supply voltage for the Op AMP
  - Set Input voltage on Vref 1 =  $V_{dd}/2$
  - Include additional voltage divider (1:1)

### Astabiler Multivibrator mit Operationsverstärker/Komparator



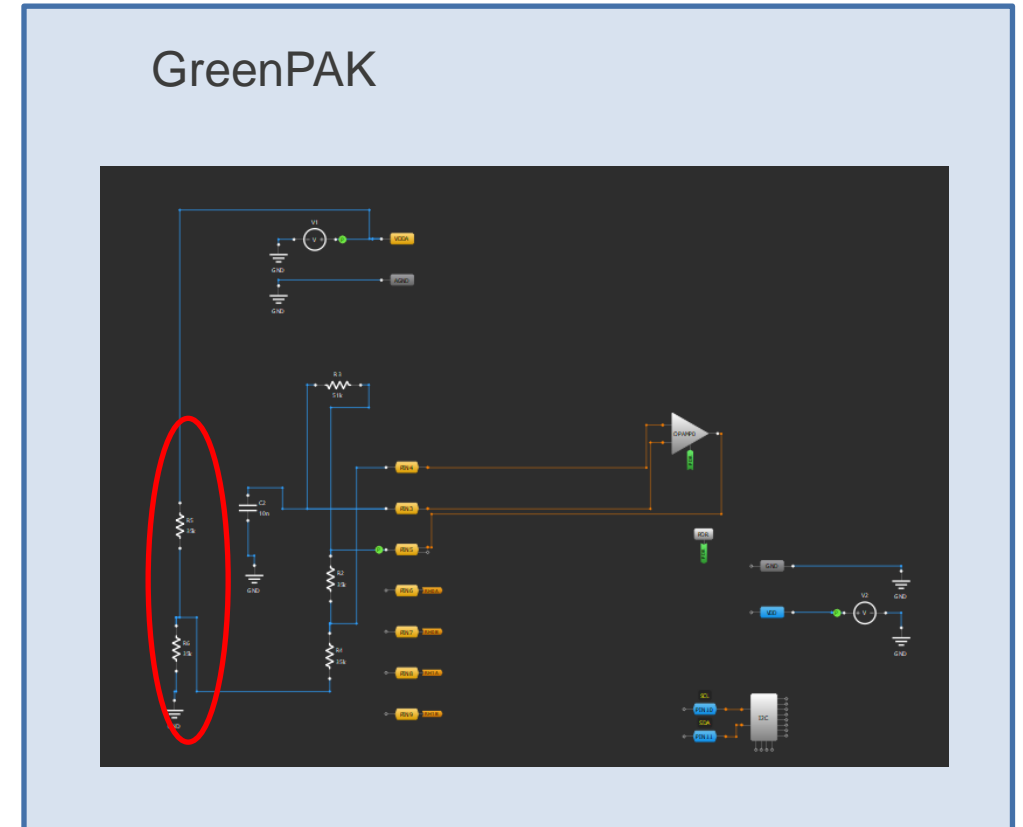
C1:  nF

R1:  kOhm

R3:  kOhm

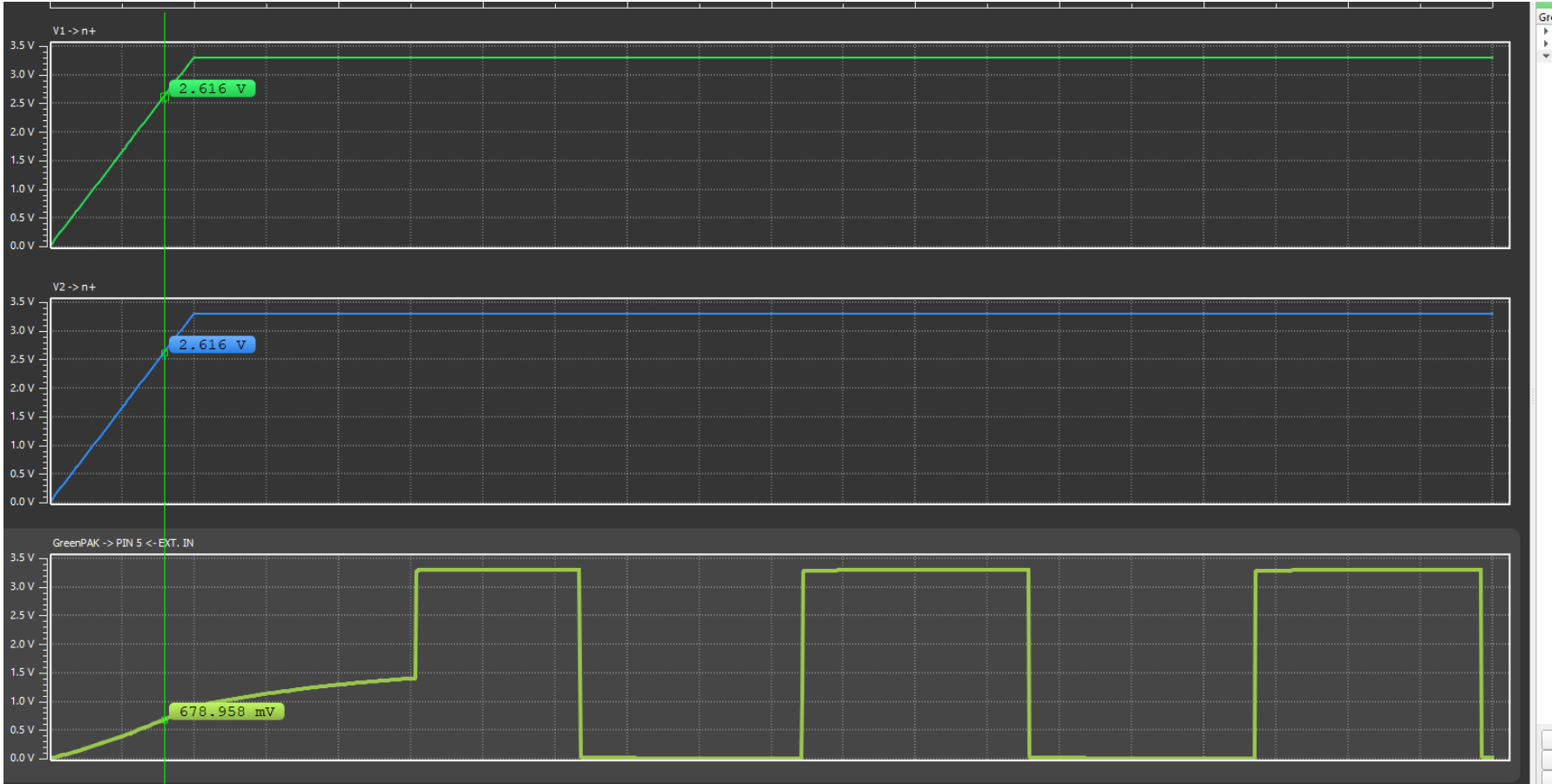
R2:  kOhm

Frequenz:  Periodendauer:



# GREENPAK APPLICATION EXAMPLES

## Multivibrator (Op Amp Design)

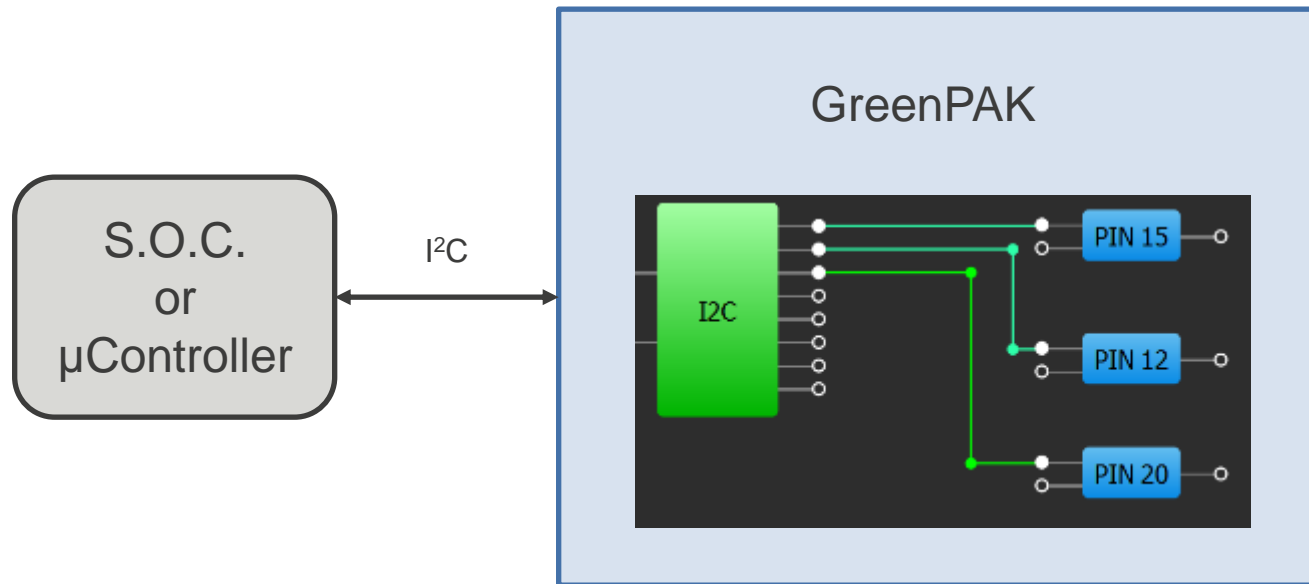




# GREENPAK APPLICATION EXAMPLES

## GPIO Expander

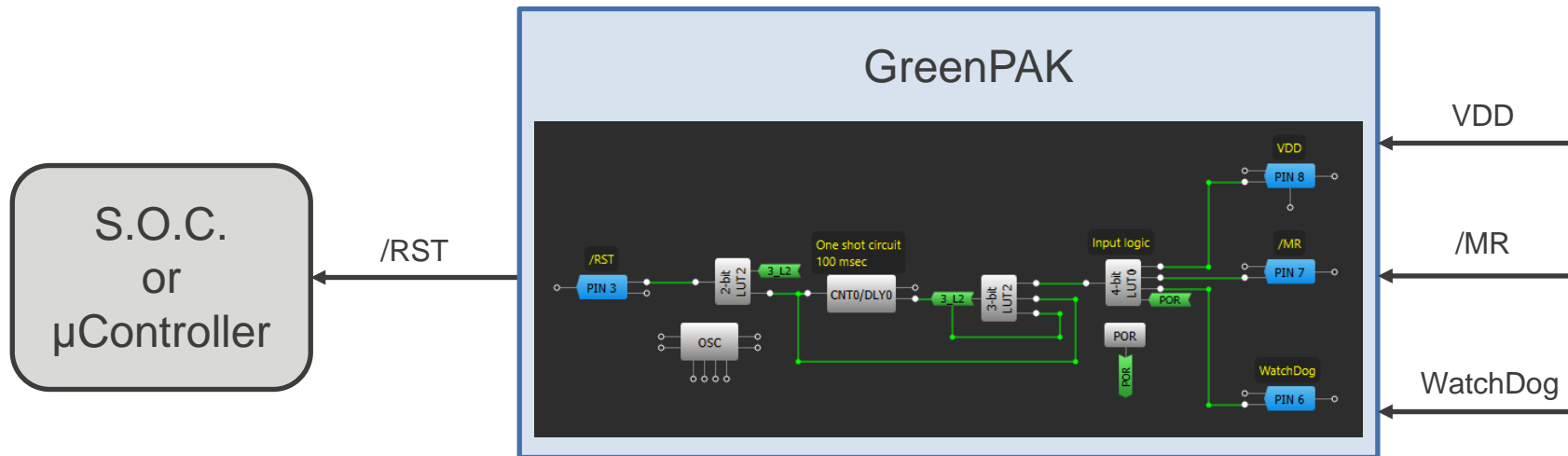
- Uses the I<sup>2</sup>C port in SLG4653xV
- Access GreenPAK pin state by a read command (up to 16 pins with SLG46533/SLG46537/SLG46538V)
- Optional /INT pin can be implemented for continuous pin monitoring



# GREENPAK APPLICATION EXAMPLES

## System Reset

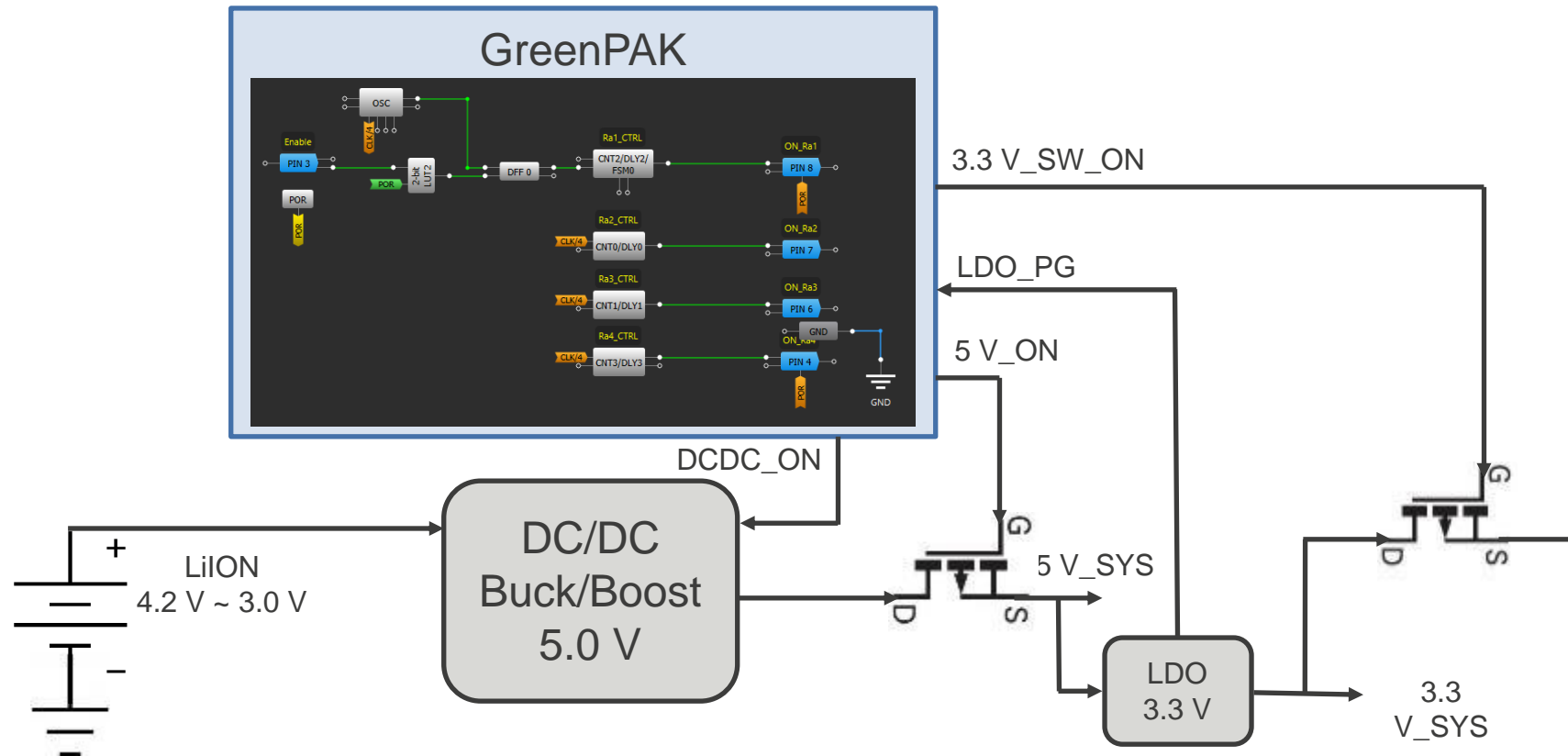
- Can be implemented in any GreenPAK silicon
- Inputs: /MR, VDD, WatchDog, voltage rail, logic signal
- Output: one shot pulse of almost any time length, level shifted logic



# GREENPAK APPLICATION EXAMPLES

## Power Rail Sequencing

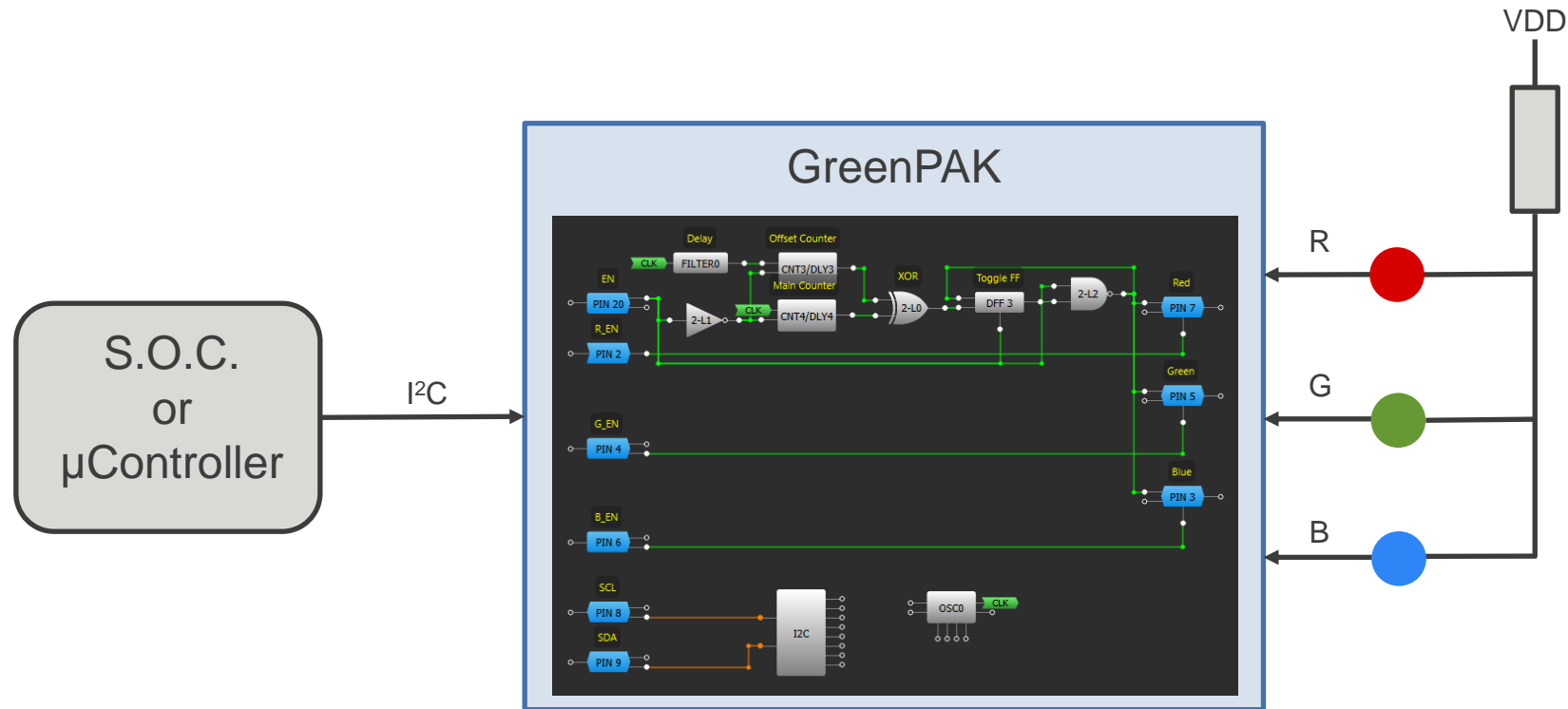
- Can be implemented in any GreenPAK silicon
- Inputs: logic signals, PGs, voltage levels
- Outputs: load switch OEs, LDO OEs, DC/DC OEs, MOSFET gates



# GREENPAK APPLICATION EXAMPLES

## RGB LED Driver

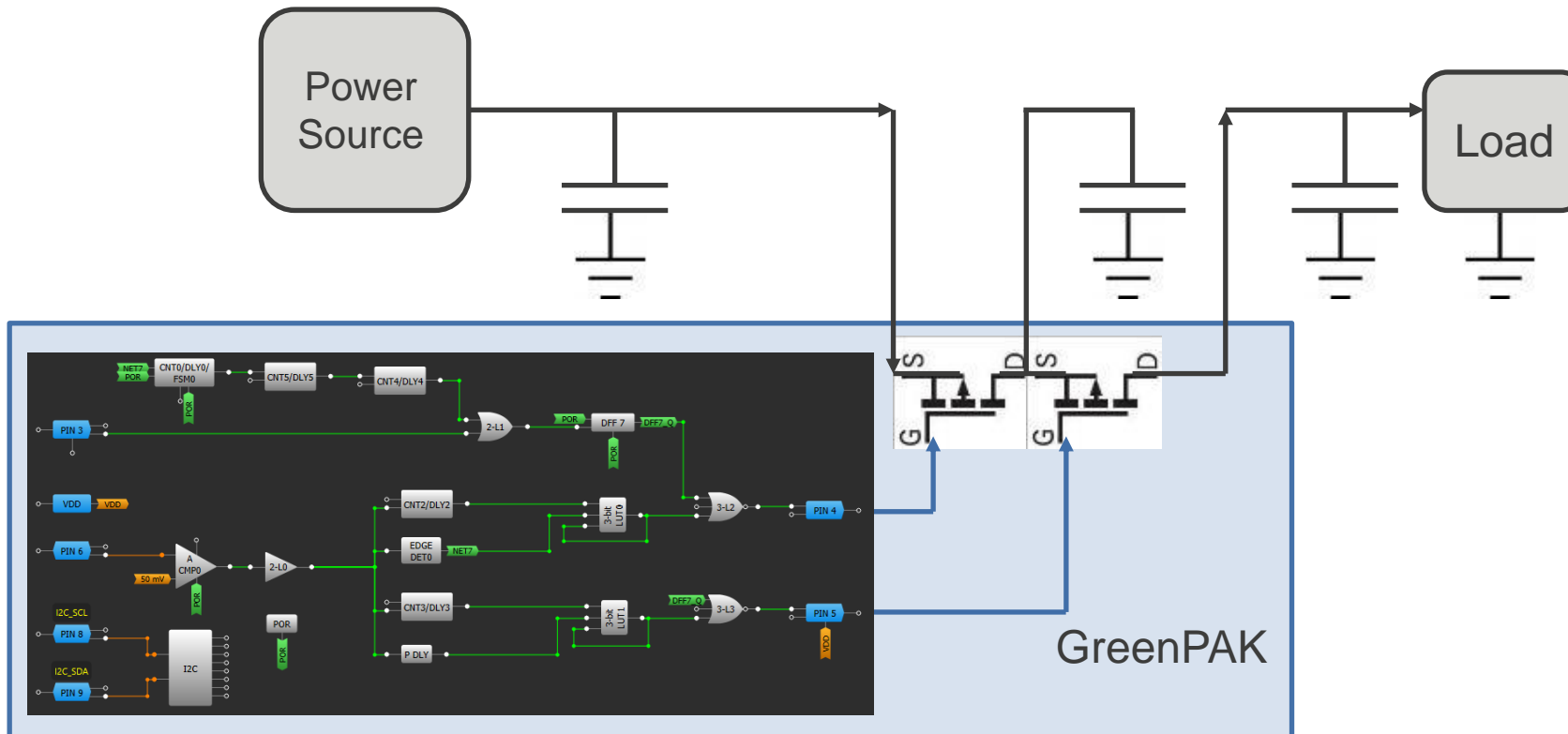
- Uses the I2C port in SLG4653xV, can be implemented with SPI in other GreenPAKs
- Inputs: write command for color, flashing time, pulsing time, breath time
- Output: PWM signal with timing to drive RGB diode(s)



# GREENPAK APPLICATION EXAMPLES

## Coulomb Counter

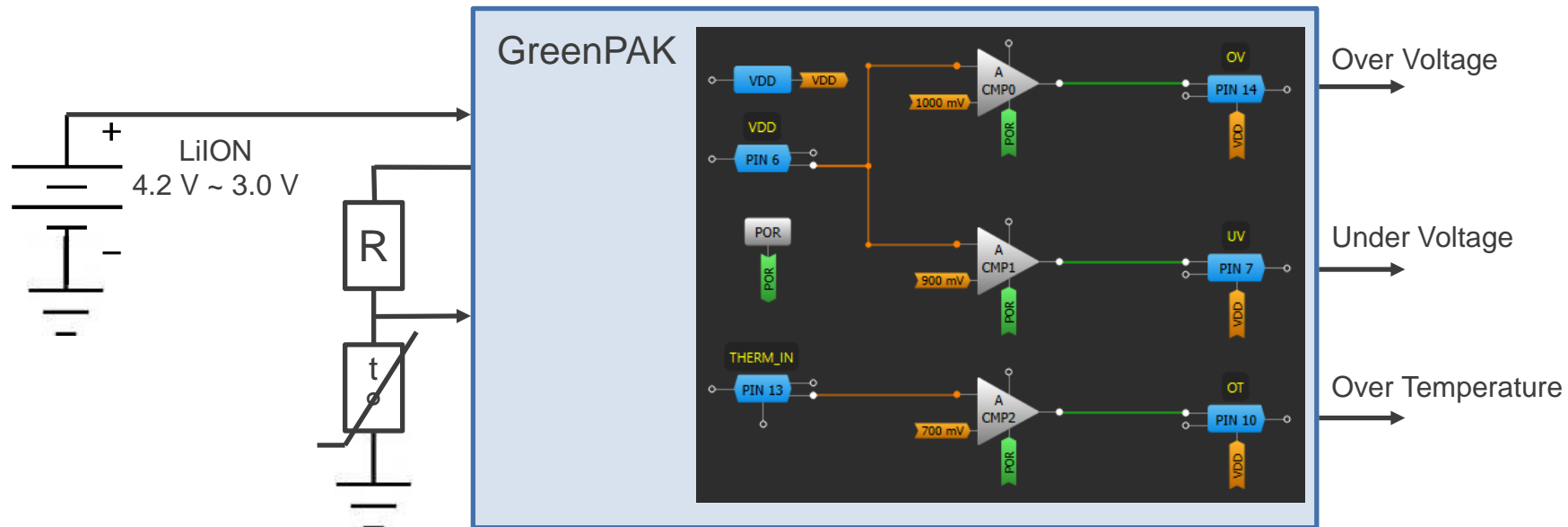
- 2 uA power consumption; linear for power switch currents from uA to mA
- Inputs: Current through power switches
- Output: Frequency proportional to current through switches or I2C counter read



# GREENPAK APPLICATION EXAMPLES

## Safety Features

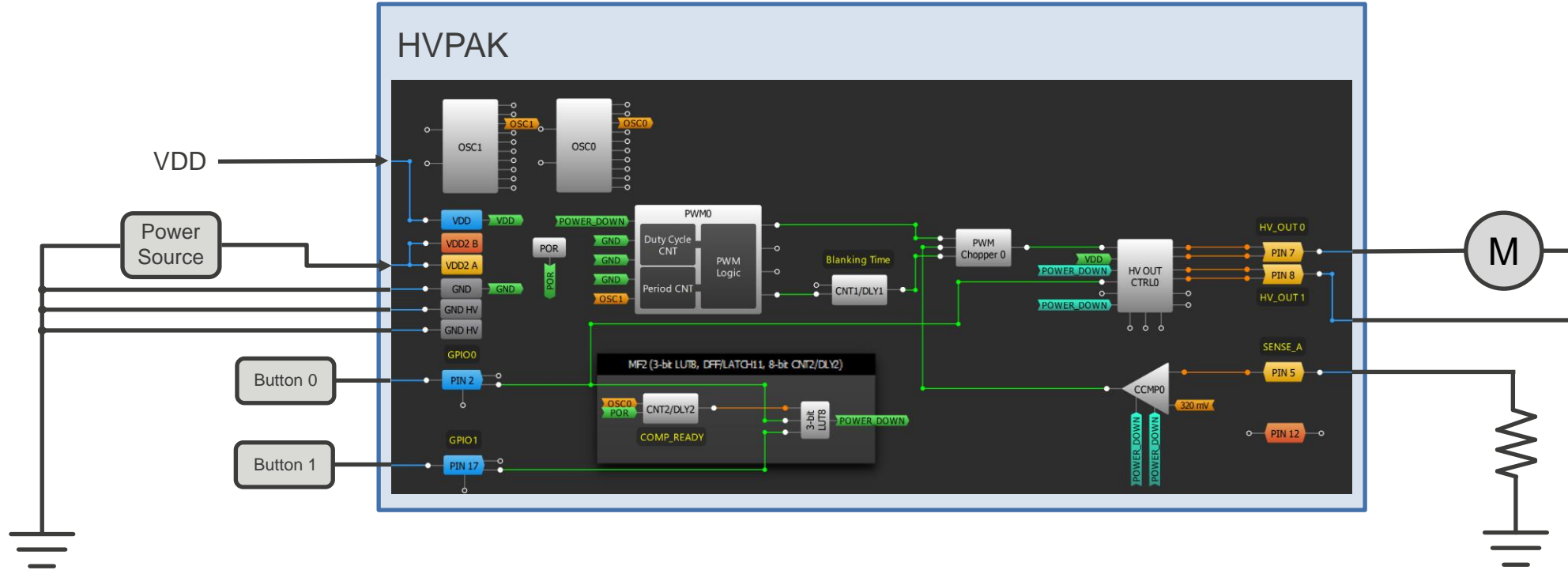
- Can be implemented in any GreenPAK silicon with ACMPs
- Inputs: VDD, voltage rails, thermistors, other sensing elements
- Outputs: over/under voltage indication, over temperature



# GREENPAK APPLICATION EXAMPLES

## HVPAK Motor Driver with Current Limiting Application

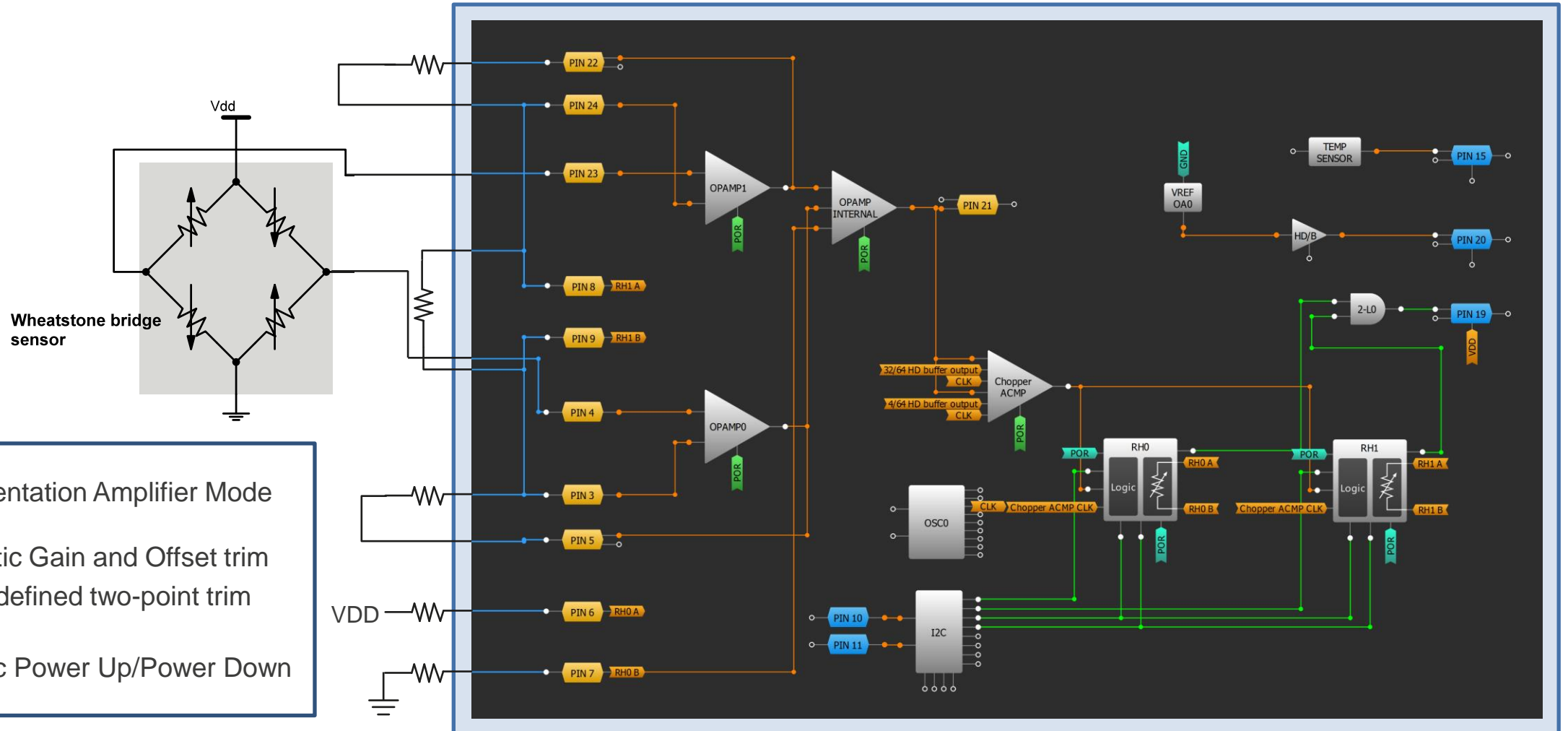
- Can be implemented using HVPAK family ICs
- Inputs: VDD, power source, two buttons
- Outputs: custom motor control with over current protection



# GREENPAK APPLICATION EXAMPLES

## Wheatstone Bridge Sensors Interface Using AnalogPAK SLG47004

AnalogPAK



- Instrumentation Amplifier Mode
- Automatic Gain and Offset trim or user-defined two-point trim
- Dynamic Power Up/Power Down



---

[Renesas.com](https://www.renesas.com)