## Features

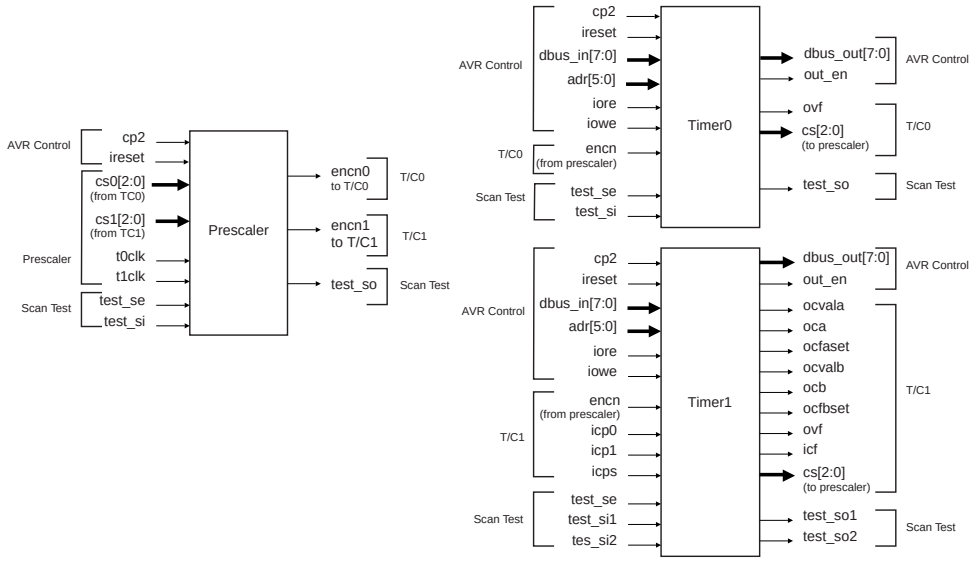
- **8- or 16-bit Timer/Counter**
- **16-bit Timer/Counter includes:**
  - **Two Output Compare Functions**
  - **One Input Capture Function**
  - **8 to 10-bit Pulse Width Modulator**
- **Individual 10-bit Prescaler**
- **Prescaled Clocking or External Clocking Schemes**
- **1.6V to 3.6V Operating Range**
- **Fully Static Operation: 0 to 33 MHz**
- **Up to 100% Fault Coverage**

## Description

The AVR® Embedded RISC Microcontroller Core is a low-power CMOS 8-bit micro-pro-cessor based on the AVR enhanced RISC architecture. With this core, Atmel supplies two general purpose Timer/Counters - one 8-bit (T/C0) and one 16-bit (T/C1).

The Timer/Counters have individual prescaling selection from the same 10-bit prescaling timer. Both Timer/Counters can either be used as a timer with an internal clock timebase or as a counter with an external pin connection which triggers the counting.

**Figure 1.** Timer/Counter Pin Configuration




Note: Standard I/Os with the same name must be connected together. Test pins however, can be connected for serial or parallel scan.

# Timer/Counter

# AVR® Embedded RISC Microcontroller Core Peripheral

Rev. 1128A–02/99

**Table 1.** Pin Description

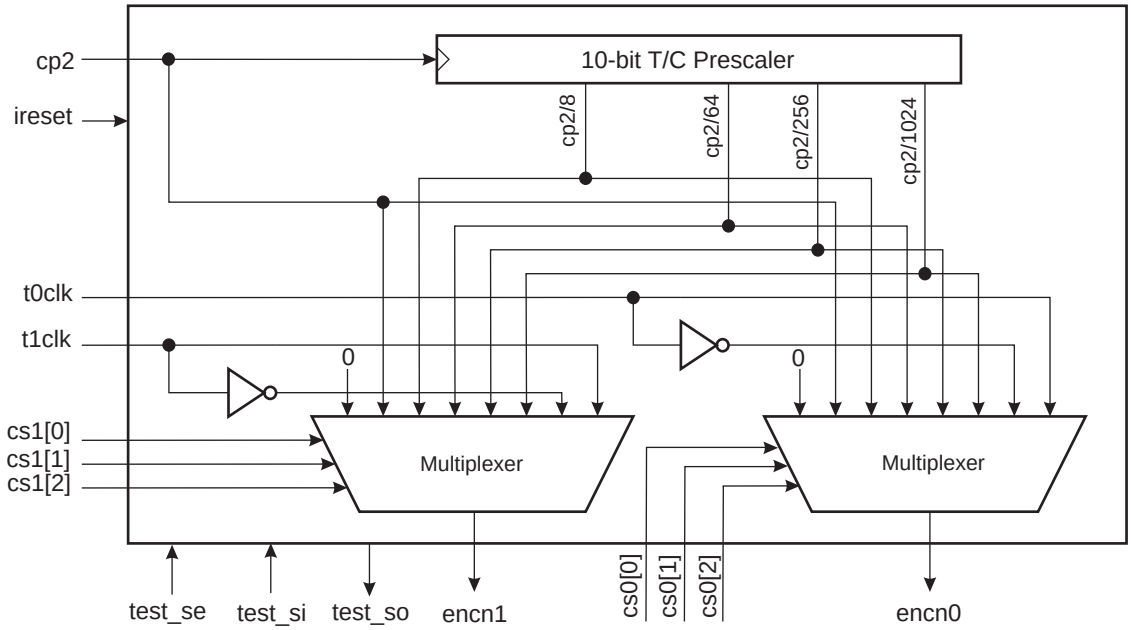
| Block | Pin Name | Description | Direction | Comments |
|---|---|---|---|---|
| Prescaler | AVR Control | | | |
| | cp2 | CPU clock | Input | All registers in Prescaler update their contents only on the positive edge of cp2 |
| | ireset | Synchronous reset | Input | When high, ireset will reset internal registers by reading the value on dbus_in which is forced to zero by the AVR Core. |
| | Prescaler | | | |
| | t0clk | Timer/Counter0 external clock | Input | External clock for T/C0, selected by cs0[2:0] |
| | t1clk | Timer/Counter1 external clock | Input | External clock for T/C1, selected by cs1[2:0] |
| | encn0 | Timer/Counter0 enable | Output | Must be connected to encn input of T/C0 |
| | encn1 | Timer/Counter1 enable | Output | Must be connected to encn input of T/C1 |
| | cs0[2:0] | Clock select input for Timer/Counter0 | Input | Must be connected to cs[2:0] output of T/C0 |
| | cs1[2:0] | Clock select input for Timer/Counter1 | Input | Must be connected to cs[2:0] output of T/C1 |
| | Scan Test | | | |
| | test_si | Test scan in | Input | |
| | test_so | Test scan out | Output | |
| | test_se | Test scan enable | Input | |
| Timer/Counter0 (T/C0) | AVR Control | | | |
| | cp2 | CPU clock | Input | All registers in T/C0 update their contents only on the positive edge of cp2 |
| | ireset | Synchronous reset | Input | When high, ireset will reset internal registers by reading the value on dbus_in which is forced to zero by the AVR Core. |
| | dbus_out[7:0] | Data bus output | Output | Valid only when accompanied by a strobe on out_en |
| | dbus_in[7:0] | Data bus input | Input | |
| | out_en | Output enable strobe | Output | When high, out_en indicates that T/C0 requires the control of the data bus |
| | adr[5:0] | I/O address inputs | Input | Valid only when accompanied by a strobe on iore or iowe |
| | iore | I/O read strobe | Input | Used to read the contents of the I/O location addressed by adr |
| | iowe | I/O write strobe | Input | Used to update the contents of the I/O location addressed by adr |
| | T/C0 | | | |
| | ovf | Overflow output | Output | When high, ovf indicates that the overflow irq must be set on the next rising edge of cp2 |
| | encn | Counter enable | Input | Must be connected to encn0 output of prescaler |
| | cs[2:0] | Clock select output | Output | Must be connected to cs0[2:0] input of the prescaler |
| | Scan Test | | | |
| | test_si | Test scan in | Input | |
| | test_so | Test scan out | Output | |
| | test_se | Test scan enable | Input | |

**Table 1.** Pin Description (Continued)

| Block | Pin Name | Description | Direction | Comments |
|---|---|---|---|---|
| Timer/Counter1 (T/C1) | AVR Control | | | |
| | cp2 | CPU clock | Input | All registers in Timer1 update their contents only on the positive edge of cp2 |
| | ireset | Synchronous reset | Input | When high, ireset will reset internal registers by reading the value on dbus_in which is forced to zero by the AVR Core. |
| | dbus_out[7:0] | Data bus output | Output | Valid only when accompanied by a strobe on out_en |
| | dbus_in[7:0] | Data bus input | Input | |
| | out_en | Output enable strobe | Output | When high, out_en indicates that T/C1 requires the control of the data bus |
| | adr[5:0] | I/O address inputs | Input | Valid only when accompanied by a strobe on iore or iowe |
| | iore | I/O read strobe | Input | Used to read the contents of the I/O location addressed by adr |
| | iowe | I/O write strobe | Input | Used to update the contents of the I/O location addressed by adr |
| | T/C1 | | | |
| | ocvala | Compare-a valid | Output | When high, ocvala indicates that the oca output is valid and that T/C1 compare mode or pwm mode is active |
| | oca | Compare-a output | Output | Valid for compare match output and pwm output |
| | ocfaset | Compare-a flag set | Output | When high, ocfaset indicates that the compare-a irq flag must be set on the next rising edge of cp2 |
| | ocvalb | Compare-b valid | Output | When high, ocvalb indicates that the oca output is valid and that T/C1 compare mode or pwm mode is active |
| | ocb | Compare-b output | Output | Valid for compare match output and pwm output |
| | ocfbset | Compare-b flag set | Output | When high, ocfbset indicates that the compare-a irq flag must be set on the next rising edge of cp2 |
| | ovf | Overflow output | Output | When high, ovf indicates that the overflow irq flag must be set on the next rising edge of cp2 |
| | icf | Input capture flag | Output | When high, indicates that the input capture irq flag must be set on the next rising edge of cp2 |
| | encn | Counter enable | Input | Must be connected to encn1 output of prescaler |
| | cs[2:0] | Clock select output | Output | Must be connected to cs1[2:0] input of the prescaler |
| | icp0 | Input capture pin0 | Input | When high, icp0 will cause T/C1 to update the capture register with the current value of the couner, only if the icps pin is low |
| | icp1 | Input capture pin1 | Input | When high, icp1 will cause T/C1 to update the capture register with the current value of the couner, only if the icps pin is high |
| | icps | Input capture pin select | Input | icps selects the current input capture pin: icp0 when low, icp1 when high |
| | Scan Test | | | |
| | test_si1/2 | Test scan inputs | Input | |
| | test_so1/2 | Test scan outputs | Output | |
| | test_se | Test scan enable | Input | |

## Timer/Counter Prescaler

**Figure 2.** Timer/Counter Prescaler.




For the two Timer/Counters, any of the following can be selected as clock sources:

- cp2 (the master clock)
- the four prescaled selections: cp2/8, cp2/64, cp2/256 and cp2/1024
- an external source (t0clk for T/C0, t1clk for T/C1)
- stop

## 8-Bit Timer/Counter0

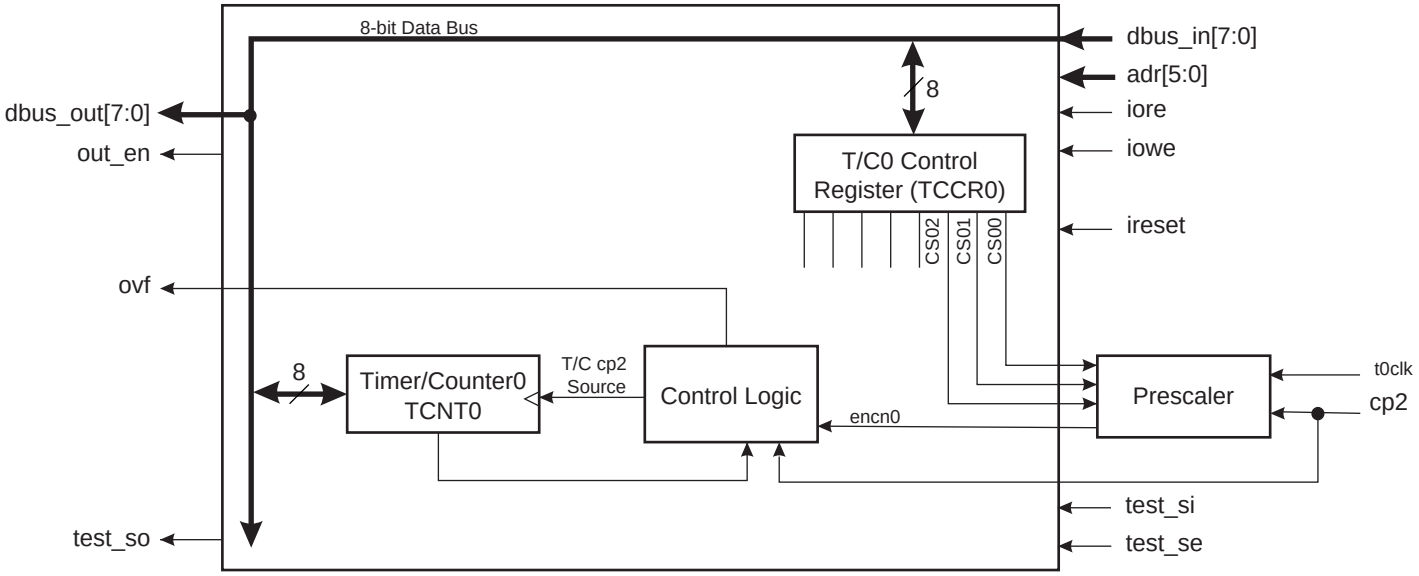
Figure 3 shows the block diagram for Timer/Counter0.

The 8-bit Timer/Counter0 can select clock source from cp2, prescaled cp2, or an external pin t0clk. In addition it can be stopped as described in the specification for the Timer/Counter0 Control Register - TCCR0. The overflow status output has to be registered in an external IRQ register. Control signals are found in the Timer/Counter0 Control Register - TCCR0.

When Timer/Counter0 is externally clocked, the external signal must be synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high resolution and a high accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

**Figure 3.** Timer/Counter0 Block Diagram



### TIMER/COUNTER0 CONTROL REGISTER - TCCR0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $33 ($53) | - | - | - | - | - | CS02 | CS01 | CS00 | TCCR0 |
| Read/Write | R | R | R | R | R | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bits 7,6,5,4,3 - Res : Reserved bits:**
These bits are reserved bits and always read zero.

**Bits 2,1,0 - CS02, CS01, CS00 : Clock Select0, bit 2,1 and 0:**
The Clock Select0 bits 2,1 and 0 define the prescaling source of Timer0.

| CS02 | CS01 | CS00 | Description |
|---|---|---|---|
| 0 | 0 | 0 | Stop, the Timer/Counter0 is stopped. |
| 0 | 0 | 1 | cp2 |
| 0 | 1 | 0 | cp2 / 8 |
| 0 | 1 | 1 | cp2 / 64 |
| 1 | 0 | 0 | cp2 / 256 |
| 1 | 0 | 1 | cp2 / 1024 |
| 1 | 1 | 0 | External Pin t0clk, falling edge |
| 1 | 1 | 1 | External Pin t0clk, rising edge |

The Stop condition provides a Timer Enable/Disable function. The cp2 divided down modes are scaled directly from the cp2 oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the data direction control register (cleared to zero gives an input pin).

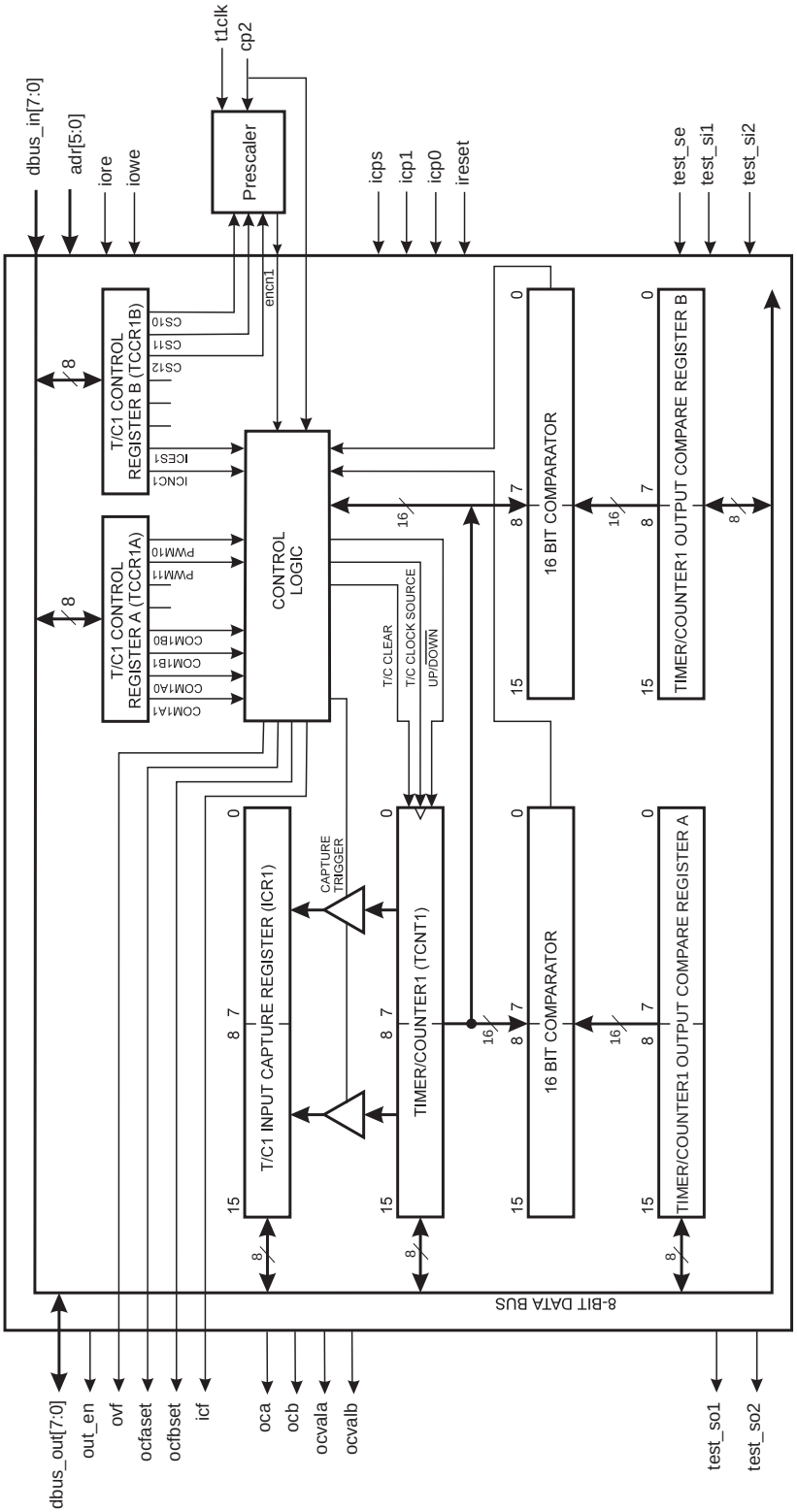
### TIMER COUNTER0 - TCNT0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $32 ($52) | MSB | | | | | | | LSB | TCNT0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

Timer/Counter0 is implemented as an up-counter with read and write access. If the Timer/Counter0 register is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.

## 16-Bit Timer/Counter1

**Figure 4.** Timer/Counter1 Block Diagram



The 16-bit Timer/Counter1 can select its clock source from cp2, prescaled cp2, or an external pin (t1clk). It can also be stopped as described in the specification for the Timer/Counter1 Control Registers - TCCR1A and TCCR1B. The different status flags (overflow, compare match and capture event) and control signals are found in the Timer/Counter1 Control Registers - TCCR1A and TCCR1B.

When Timer/Counter1 is externally clocked, the external signal must be synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 16-bit Timer/Counter1 features both a high resolution and a high accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities makes the Timer/Counter1 useful for lower speed functions or exact timing functions with infrequent actions.

The Timer/Counter1 supports two Output Compare functions using the Output Compare Register 1 A and B - OCR1A and OCR1B - as the data sources to be compared to the Timer/Counter1 contents. The Output Compare functions include optional clearing of the counter on compareA match, and actions on the Output Compare pins on both compare matches.

Timer/Counter1 can also be used as a 8, 9 or 10-bit Pulse With Modulator. In this mode the counter and the OCR1A/OCR1B registers serve as a dual glitch-free stand-alone PWM with centered pulses. Refer to Page page 13 for a detailed description on this function.

The Input Capture function of Timer/Counter1 provides a capture of the Timer/Counter1 contents to the Input Capture Register - ICR1, triggered by an external event on the Input Capture Pins - ICP0 or ICP1. The actual capture event settings are defined by the Timer/Counter1 Control Register - TCCR1B. The ICPx pin logic is shown in the figure below.

**Figure 5.** ICPx Pin Schematic Diagram

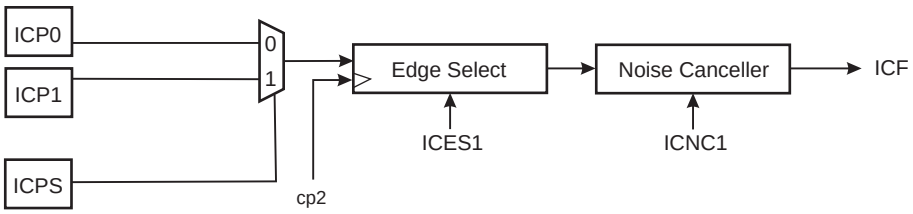
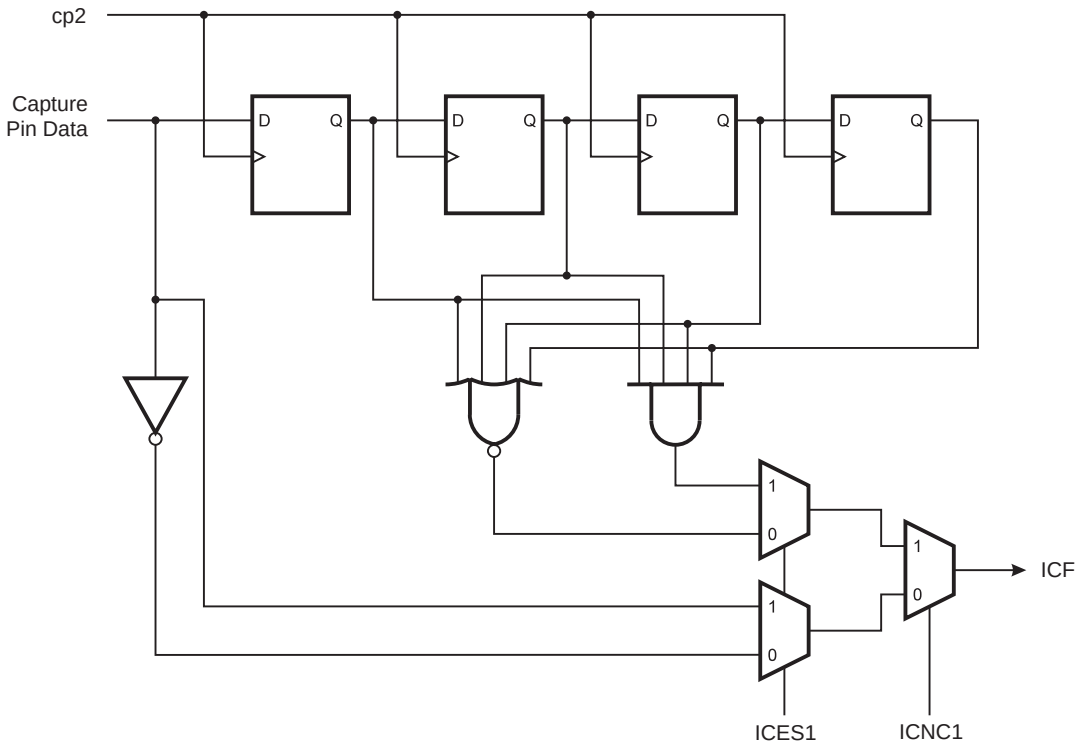


**Figure 6.** The Input Capture Noise Canceler




If the noise canceler function is enabled, the actual trigger condition for the capture event is monitored over 4 samples before the capture is activated. The input pin signal is sampled at cp2 clock frequency.

### TIMER/COUNTER1 CONTROL REGISTER A - TCCR1A

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $2F ($4F) | **COM1A1** | **COM1A0** | **COM1B1** | **COM1B0** | **-** | **-** | **PWM11** | **PWM10** | **TCCR1A** |
| Read/Write | R/W | R/W | R/W | R/W | R | R | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bits 7,6 - COM1A1, COM1A0 : Compare Output Mode1A, bits 1 and 0:**
The COM1A1 and COM1A0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OCA - Output CompareA. Since this is an alternative function to an I/O port, the corresponding direction control bit must be set (one) to control an output pin. The control configuration is shown in Table .

**Bits 5,4 - COM1B1, COM1B0 : Compare Output Mode1B, bits 1 and 0:**
The COM1B1 and COM1B0 control bits determine any output pin action following a compare match in Timer/Counter1. Any output pin actions affect pin OCB - Output CompareB. Since this is an alternative function to an I/O port, the corresponding direction control bit must be set (one) to control an output pin. The following control configuration is given:

**Table 2.** Compare 1 Mode Select

| COM1X1 | COM1X0 | Description |
|---|---|---|
| 0 | 0 | Timer/Counter1 disconnected from output pin OCX |
| 0 | 1 | Toggle the OCX output line. |
| 1 | 0 | Clear the OCX output line (to zero). |
| 1 | 1 | Set the OCX output line (to one). |

Note: X = A or B

In PWM mode, these bits have a different function. Refer to Figure for a detailed description.

When changing the COM1X1/COM1X0 bits, Output Compare Interrupts 1 must be disabled by clearing their Interrupt Enable bits the corresponding external IRQ register. Otherwise an interrupt can occur when the bits are changed.

**Bits 3..2 - Res : Reserved bits:**
These bits are reserved bits and always read zero.

**Bits 1..0 - PWM11, PWM10: Pulse Width Modulator Select Bits:**
These bits select PWM operation of Timer/Counter1 as specified in Table . This mode is described on page 13.

**Table 3.** PWM Mode Select

| PWM11 | PWM10 | Description |
|---|---|---|
| 0 | 0 | PWM operation of Timer/Counter1 is disabled |
| 0 | 1 | Timer/Counter1 is an 8-bit PWM |
| 1 | 0 | Timer/Counter1 is a 9-bit PWM |
| 1 | 1 | Timer/Counter1 is a 10-bit PWM |

### THE TIMER/COUNTER1 CONTROL REGISTER B - TCCR1B

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---|---|---|---|---|---|---|---|---|---|
| $2E ($4E) | **ICNC1** | **ICES1** | **-** | **-** | **CTC1** | **CS12** | **CS11** | **CS10** | **TCCR1B** |
| Read/Write | R/W | R/W | R | R | R/w | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

**Bit 7 - ICNC1 : Input Capture1 Noise Canceler (4 cp2s):**
When the ICNC1 bit is cleared (zero), the input capture trigger noise canceler function is disabled. The input capture is triggered at the first rising/falling edge sampled on the ICPx - input capture pin - as specified. When the ICNC1 bit is set (one), four successive samples are measures on the ICPx - input capture pin, and all samples must be high/low according to the input capture trigger specification in the ICES1 bit. The actual sampling frequency is cp2 clock frequency.

**Bit 6 - ICES1 : Input Capture1 Edge Select:**
While the ICES1 bit is cleared (zero), the Timer/Counter1 contents are transferred to the Input Capture Register - ICR1 - on the falling edge of the selected input capture pin - ICPx. While the ICES1 bit is set (one), the Timer/Counter1 contents are transferred to the Input Capture Register - ICR1 - on the rising edge of the input capture pin - ICPx.

**Bits 5, 4 - Res : Reserved bits:**
These bits are reserved bits and always read zero.

**Bit 3 - CTC1 : Clear Timer/Counter1 on Compare match:**
When the CTC1 control bit is set (one), the Timer/Counter1 is reset to $0000 in the clock cycle after a compareA match. If the CTC1 control bit is cleared, the Timer/Counter1 continues counting until it is stopped, cleared, wraps around (overflow) or changes direction. In PWM mode, this bit has no effect.

**Bits 2,1,0 - CS12, CS11, CS10 : Clock Select1, bit 2,1 and 0:**
The Clock Select1 bits 2,1 and 0 define the prescaling source of Timer/Counter1.

**Table 4.** Clock 1 Prescale Select

| CS12 | CS11 | CS10 | Description |
|---|---|---|---|
| 0 | 0 | 0 | Stop, the Timer/Counter1 is stopped. |
| 0 | 0 | 1 | cp2 |
| 0 | 1 | 0 | cp2 / 8 |
| 0 | 1 | 1 | cp2 / 64 |
| 1 | 0 | 0 | cp2 / 256 |
| 1 | 0 | 1 | cp2 / 1024 |
| 1 | 1 | 0 | External Pin t1clk, falling edge |
| 1 | 1 | 1 | External Pin t1clk, rising edge |

The Stop condition provides a Timer Enable/Disable function. The cp2 down divided modes are scaled directly from the cp2 oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the actual direction control register (cleared to zero gives an input pin).

**TIMER/COUNTER1 - TCNT1H AND TCNT1L**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| $2D ($4D) | **MSB** | | | | | | | | **TCNT1H** |
| $2C ($4C) | | | | | | | | **LSB** | **TCNT1L** |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

This 16-bit register contains the current value of the 16-bit Timer/Counter1. To ensure that both the high and low bytes are read and written simultaneously when the CPU accesses these registers, the access is performed using an 8-bit temporary register (TEMP).

- **TCNT1 Timer/Counter1 Write:**

  When the CPU writes to the high byte TCNT1H, the written data is placed in the TEMP register. Next, when the CPU writes the low byte TCNT1L, this byte of data is combined with the byte data in the TEMP register, and all 16 bits are written to the TCNT1 Timer/Counter1 register simultaneously. Consequently, the high byte TCNT1H must be accessed first for a full 16-bit register write operation.

- **TCNT1 Timer/Counter1 Read:**

  When the CPU reads the low byte TCNT1L, the data of the low byte TCNT1L is sent to the CPU and the data of the high byte TCNT1H is placed in the TEMP register. When the CPU reads the data in the high byte TCNT1H, the CPU receives the data in the TEMP register. Consequently, the low byte TCNT1L must be accessed first for a full 16-bit register read operation.

Timer/Counter1 is implemented as an up or up/down (in PWM mode) counter with read and write access. If Timer/Counter1 is written to and a clock source is selected, the Timer/Counter1 continues counting in the timer clock cycle after it is preset with the written value.

### TIMER/COUNTER1 OUTPUT COMPARE REGISTER - OCR1AH AND OCR1AL

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| $2B ($4B) | **MSB** | | | | | | | | **OCR1AH** |
| $2A ($4A) | | | | | | | | **LSB** | **OCR1AL** |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

### TIMER/COUNTER1 OUTPUT COMPARE REGISTER - OCR1BH AND OCR1BL

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| $29 ($49) | **MSB** | | | | | | | | **OCR1BH** |
| $28 ($48) | | | | | | | | **LSB** | **OCR1BL** |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

The output compare registers are 16-bit read/write registers.

The Timer/Counter1 Output Compare Registers contain the data to be continuously compared with Timer/Counter1. Actions on compare matches are specified in the Timer/Counter1 Control and Status register.

Since the Output Compare Registers - OCR1A and OCR1B - are 16-bit registers, a temporary register TEMP is used when OCR1A/B are written to ensure that both bytes are updated simultaneously. When the CPU writes the high byte, OCR1AH or OCR1BH, the data is temporarily stored in the TEMP register. When the CPU writes the low byte, OCR1AL or OCR1BL, the TEMP register is simultaneously written to OCR1AH or OCR1BH. Consequently, the high byte OCR1AH or OCR1BH must be written first for a full 16-bit register write operation.

### TIMER/COUNTER1 INPUT CAPTURE REGISTER - ICR1H AND ICR1L

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
|---|---|---|---|---|---|---|---|---|---|
| $27 ($47) | **MSB** | | | | | | | | **ICR1H** |
| $26 ($46) | | | | | | | | **LSB** | **ICR1L** |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Read/Write | R | R | R | R | R | R | R | R | |
| | R | R | R | R | R | R | R | R | |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

The input capture register is a 16-bit read-only register.

When the rising or falling edge (according to the input capture edge setting - ICES1) of the signal at the selected input capture pin - ICPx - is detected, the current value of the Timer/Counter1 is transferred to the Input Capture Register - ICR1. At the same time, the input capture flag - ICF - is set (one).

Since the Input Capture Register - ICR1 - is a 16-bit register, a temporary register TEMP is used when ICR1 is read to ensure that both bytes are read simultaneously. When the CPU reads the low byte ICR1L, the data is sent to the CPU and the data of the high byte ICR1H is placed in the TEMP register. When the CPU reads the data in the high byte ICR1H, the CPU receives the data in the TEMP register. Consequently, the low byte ICR1L must be accessed first for a full 16-bit register read operation.

**Timer/Counter1 in PWM Mode**

When the PWM mode is selected, Timer/Counter1 and the Output Compare Register1A - OCR1A and the Output Compare Register1B - OCR1B, form a dual 8, 9 or 10-bit, free-running, glitch-free and phase correct PWM with outputs on the OCA and OCB pins. Timer/Counter1 acts as an up/down counter, counting up from $0000 to TOP (see Table ) , when it turns and counts down again to zero before the cycle is repeated. When the counter value matches the contents of the 10 least significant bits of OCR1A or OCR1B, the OCA/OCB pins are set or cleared according to the settings of the COM1A1/COM1A0 or COM1B1/COM1B0 bits in the Timer/Counter1 Control Register TCCR1A. Refer to Table  for details.

**Table 5.** Timer TOP Values and PWM Frequency

| PWM Resolution | Timer TOP value | Frequency |
|---|---|---|
| 8-bit | $00FF (255) | $f_{TC1}/510$ |
| 9-bit | $01FF (511) | $f_{TC1}/1022$ |
| 10-bit | $03FF(1023) | $f_{TC1}/2046$ |

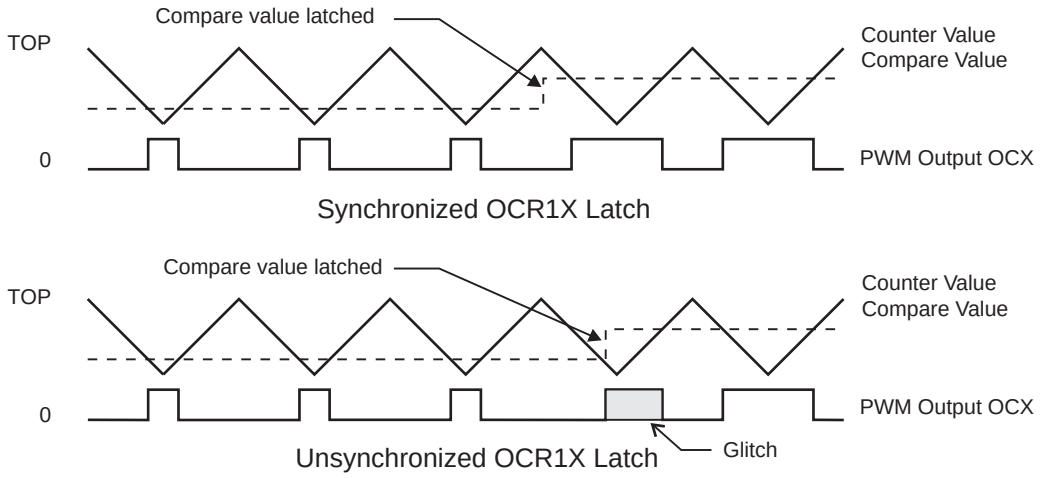
**Table 6.** Compare1 Mode Select in PWM Mode

| COM1X1 | COM1X0 | Effect on OCX1 |
|---|---|---|
| 0 | 0 | Not connected |
| 0 | 1 | Not connected |
| 1 | 0 | Cleared on compare match, upcounting. Set on compare match, downcounting (non-inverted PWM). |
| 1 | 1 | Cleared on compare match, downcounting. Set on compare match, upcounting (inverted PWM). |

Note: X = A or B

Note that in the PWM mode, the 10 least significant OCR1A/OCR1B bits, when written, are transferred to a temporary location. They are latched when Timer/Counter1 reaches the value TOP. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR1A/OCR1B write. See Figure 7 for an example.

**Figure 7.** Effects on Unsynchronized OCR1 Latching




Note: X = A or B

When OCR1 contains $0000 or TOP, the output OCA/OCB is held low or high according to the settings of COM1A1/COM1A0 or COM1B1/COM1B0. This is shown in Table :

**Table 7.** PWM Outputs OCR1X = $0000 or TOP

| COM1X1 | COM1X0 | OCR1X | **Output OCX** |
|---|---|---|---|
| 1 | 0 | $0000 | L |
| 1 | 0 | TOP | H |
| 1 | 1 | $0000 | H |
| 1 | 1 | TOP | L |

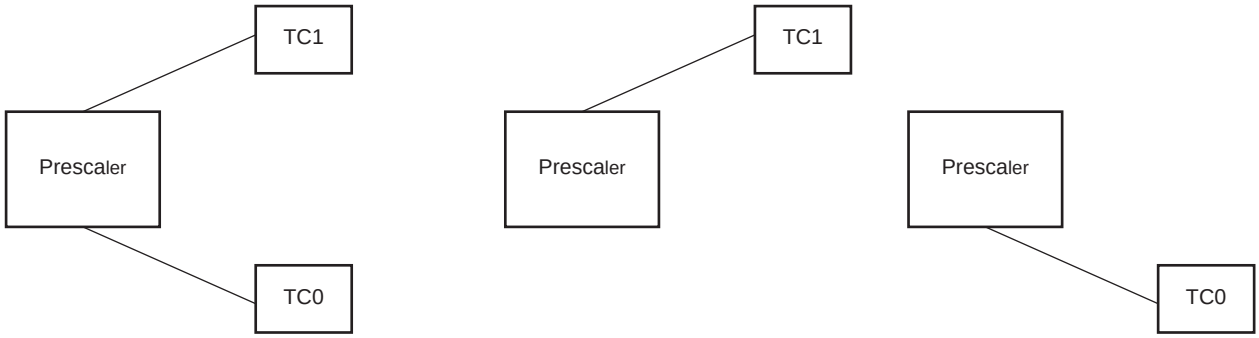
Note: X = A or B

In PWM mode, the Timer Overflow Flag1 (OVF) is set when the counter changes direction at $0000. Timer Overflow Interrupt operates exactly as in normal Timer/Counter mode.

## Block Configuration

The three blocks (Timer0, Timer1, Prescaler) can be connected in the following ways:

**Figure 8.** Block Configuration




For all other configurations, the Timer/Counter block which is used two times or more must be resynthesized to change its internal addresses.

## Scan Test Configuration

The AVR Timer/Counter standard peripheral has been designed with a full scan methodology which results in a 100% maximum fault coverage.

The coverage is maximum if all non-scan inputs can be controlled and all non-scan outputs can be observed. In order to acheive this, the ATPG vectors must be generated on the entire circuit (top level) which includes the AVR Timer/Counter.

The scan test pins can then be connected for serial or parallel scan.

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